

THE **pcb** **design** MAGAZINE

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IPC-A-610: What's New
with Rev F?

p.16

PLUS:

Rigid-Flex PCB Right
the First Time—Without
Paper Dolls

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IPC 610 UPDATE

The Past, Present, and Future of IPC-A-610

By Teresa Rowe, page 10

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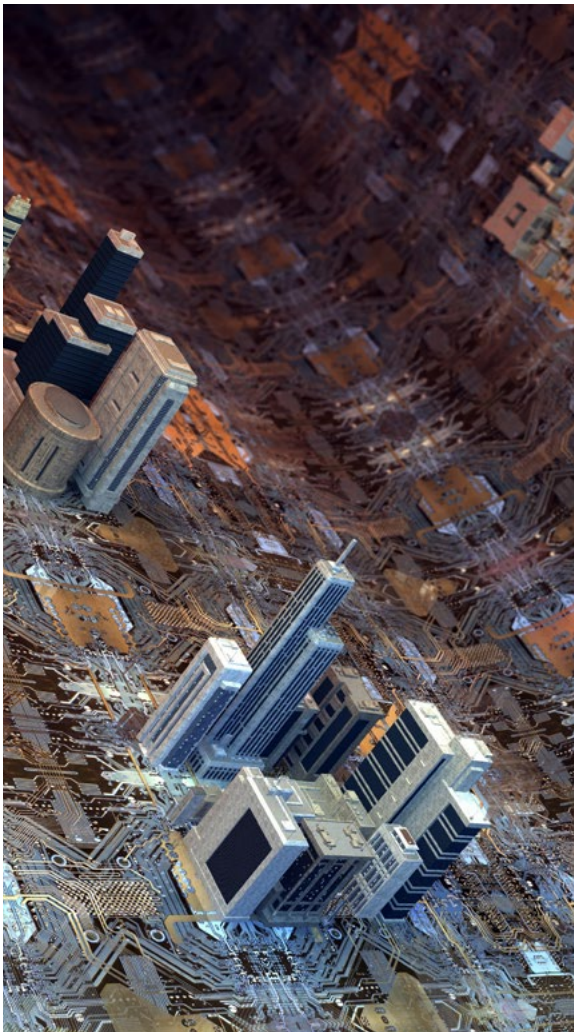
This Issue: IPC 610 UPDATE

FEATURED CONTENT

IPC-A-610, *Acceptability of Electronic Assemblies* is the most widely used IPC standard. This month our expert contributors Teresa Rowe of IPC and Leo Lambert of EPTAC discuss the latest updates to this document, what they mean to product developers, and the various steps in the revision process itself.

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by Leo Lambert





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Df @ 10 GHz	0.0028 - 0.0036	0.0028, 0.0031 & 0.0034	0.0031*	0.0030*	0.0017
CTE Z-axis (50 to 260°C)	2.90%	2.80%	2.80%	2.90%	2.90%
T-260 & T-288	>60	>60	>60	>60	>60
Halogen free	No	No	No	Yes	No
VLP-2 (2 micron Rz copper)	Available	Available	Available	Standard	Standard
Stable Dk & Df over the temperature range	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-40°C to +140°C
Optimized global constructions for Pb-free assembly	Yes	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	For use in double-sided applications	Yes	Yes	Yes	Yes
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* Dk & Df are dependent on resin content NOTE: Dk/Df is at one resin %. Please refer to the Isola website for a complete list of Dk/Df values. The data, while believed to be accurate & based on analytical methods considered to be reliable, is for information purposes only. Any sales of these products will be governed by the terms & conditions of the agreement under which they are sold.

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<https://isodesign.isola-group.com/phi-calculator>

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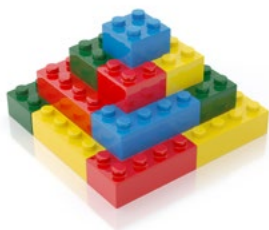
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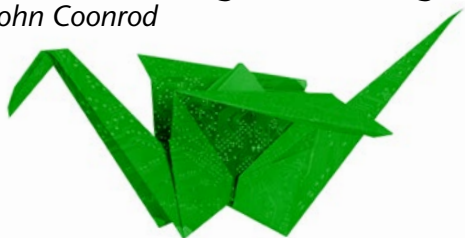


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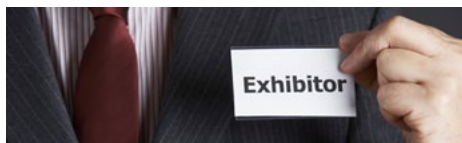
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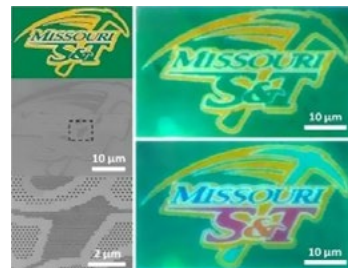
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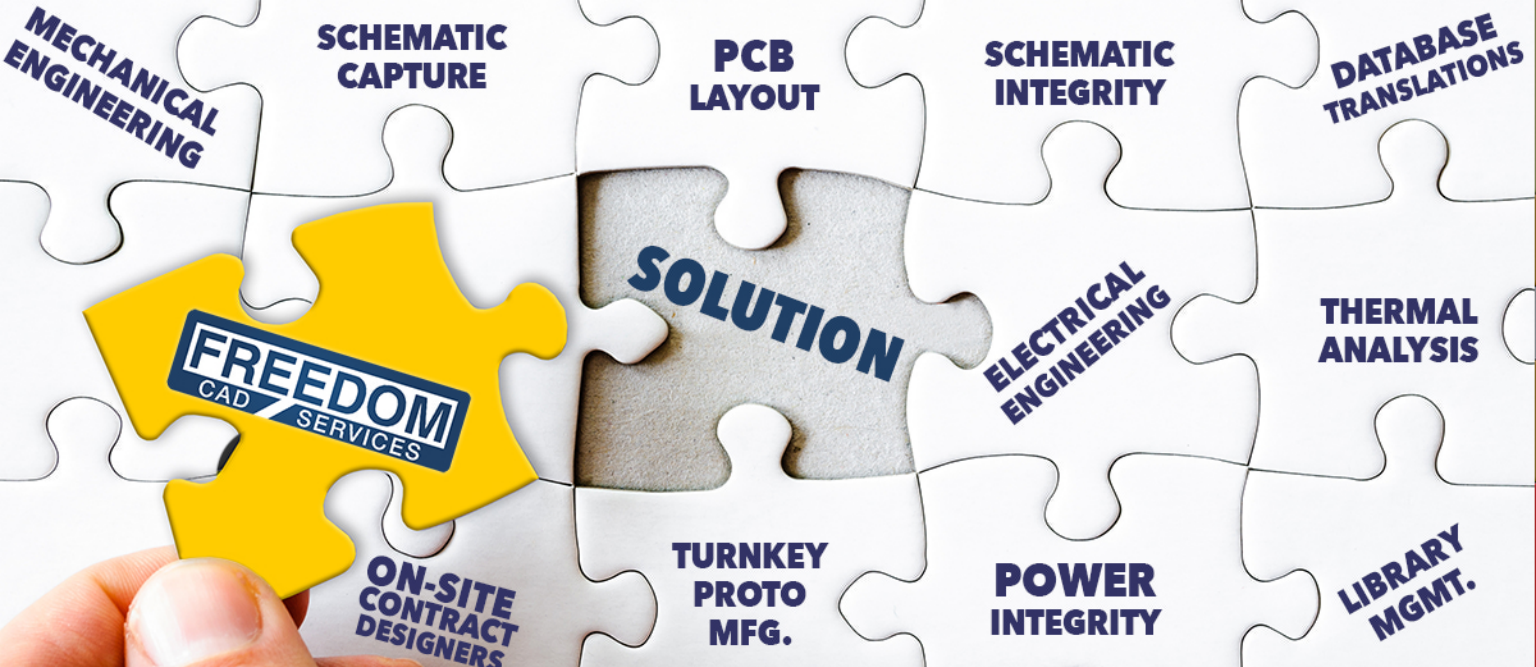


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Imagine that you support a few PCB designers working on cutting-edge applications that utilize RF, microwave, and other high-speed design technologies. Some of you may fit this description.

Now, imagine you're supporting 1,700 designers across 50 countries, speaking a variety of languages. Monica Andrei of the Germany-based Continental Automotive Systems doesn't have to imagine; for her, that's just a typical day at the office—if you can call that typical.

Andrei was one of the speakers at Zuken Innovation World (ZIW), held June 1–3 at the Coronado Island Marriott Resort and Spa in San Diego. This annual event draws Zuken designers and engineers from every segment of the electronics industry. Zuken usually picks a nice venue for their events, but Coronado Island is pretty much unbeatable. It was 70 degrees on the water, with a good breeze blowing. If you have to work, Coronado Island is the place to be! Big thanks to Zuken's Amy Clements for putting this whole thing together.

Continental develops electronic systems, tires, fuel injection systems and more for many of the world's car and truck makers, including all of the German companies, General Mo-

tors, Ford, Honda, Toyota, Renault, Iveco, and Freightliner Trucks. Andrei, now based in Detroit, joked about the logistics involved in supporting 1,700 PCB designers and engineers in so many countries and time zones. Continental had €34 billion in sales last year.

The automotive, military, and aerospace segments make up a good chunk of Zuken's market share. Technologists from these areas and more were all represented at ZIW. As in years past, when the event was known as ZDAC, I ran into dozens of Zuken users who really love their tools. And I don't mean the normal love/hate relationship many of you have with your tools. Most designers tell me, "I love how my software does X and Y, but the way it does Z makes me pull out what's left of my hair. I wish my EDA company would listen to me."

At ZIWI, I met designers and engineers who raved about their tools, like classic car nuts at a Mustang show. And they also feel that Zuken really does listen to their complaints and comments about the tools. Over the years, I've asked the Zuken folks about this, and they said they just try to listen to their users. It's nothing fancier than that, but it seems to be working.

How many of you go around bragging about your software tools and customer support?





Julie Ellis, TTM Technologies (left) and Matt Isaacs, Broadcom (right) speak at the Orange County Designers Council meeting.

On to the Designers Council Meeting

Next, I fired up my trusty Hyundai rental car and headed north to Orange County for a Designers Council lunch-and-learn. (When did Hyundais become such good cars? I rented one once and I had to push it uphill. Not so with this rocket Elantra.)

Though he's not a designer by trade, you'd never know it from talking to Scott McCurdy, longtime president of the Orange County Chapter of the Designers Council and director of sales and marketing for Freedom CAD. Yes, McCurdy has been a fabricator for decades, but he's also a big champion for PCB design and designers. As chapter prez, he's mastered the art of herding cats; the DC meeting on June 3 at Broadcom's UC Irvine campus drew over 100 people.

The first speaker was Matt Isaacs, technical director at Broadcom. He discussed a qualification vehicle that Broadcom had fabricated. His team sent the same PCB design to five different fabricators, without providing any special directions.

His group then put the resulting boards through a series of electrical tests, and found that every single board was completely different.

"We saw very little difference with TDR looking at just impedance. Trace impedance with TDR...everything looked pretty good," said Isaacs. "But once we got to the VNA, [vector network analyzer], looking at attenuation vs. frequency, we really started to see a lot of surprising data. For some fabs, certain layers were great and other layers were problematic."

But the Number 1 problem for all five fabricators was the via. Isaacs' presentation included information on tuning vias by using antipads and backdrilling. One of the bullet points read, "There's no such thing as a good, partially back-

drilled via." Isaacs found that basic PCBA construction works fine up to 28 Gbps and beyond.

Next up was Julie Ellis, a field application engineer for TTM Technologies and 30-year industry veteran. Her presentation also focused on vias, and how tough it is to get consistent plating into a blind via, or in a 6 mil via that's three times the thickness of a human hair. Ellis explained how reverse pulse plating works, and why that's often the best choice for achieving uniform coverage in vias.

Ellis noted that TTM won't use mechanical drills for any pitch below .8 mils, so they use YAG or CO₂ lasers instead, or a combination of the two: YAG can pierce copper and dielectric, while CO₂ bounces off copper. Ellis explained that any vias smaller than .8 mils generally can't be built in China.

Ellis also discussed a TTM technology used for fanning out from large BGAs: next-generation SMV, or stacked microvias. These BGAs with thousands of pins were almost impossible to fanout, but with SMV, each pin in the BGA has its own layer, connected by microvia. It looks like a nightmare to fabricate, though.

Another big thank you to Scott McCurdy for inviting me to his OC lunch-and-learn. He said he used to get five attendees; now he has about 100 most of the time. I'd be happy to come back some day! **PCBDESIGN**



Andy Shaughnessy is managing editor of *The PCB Design Magazine*. He has been covering PCB design for 15 years. He can be reached by clicking [here](#).



The Past, Present, and Future of IPC-A-610

By Teresa Rowe
IPC


IPC-A-610 At-a-Glance

Since 1983, IPC-A-610, *Acceptability of Electronic Assemblies*, has been the standard used by organizations interested in understanding the acceptability criteria for electronic assemblies around the world.

To understand the ultimate power of IPC-A-610, you need to first understand what is at the core of this standard. IPC-A-610 is a collection of visual quality acceptability requirements for electronic assemblies. It is utilized as a post-assembly acceptance standard to ensure that electronic assemblies meet acceptance requirements.

IPC-A-610 is an essential document in an electronic assembler's library. Not only is it necessary to have the proper material and tools, but it is also important to have clearly defined acceptance criteria. IPC-A-610 provides that criteria developed and accepted by representatives from some of our industry's leaders.

Most often, IPC-A-610 is used as a companion document to other standards. While there is much overlap in criteria for these compatible standards, each has a unique purpose. The development and evolution of IPC-A-610 falls largely on a unified task group, which consists of volunteers who often work together on other standards as well. It is because of this that so many standards are able to operate as companion pieces. For example, IPC J-STD-001 is a material and process requirements standard that



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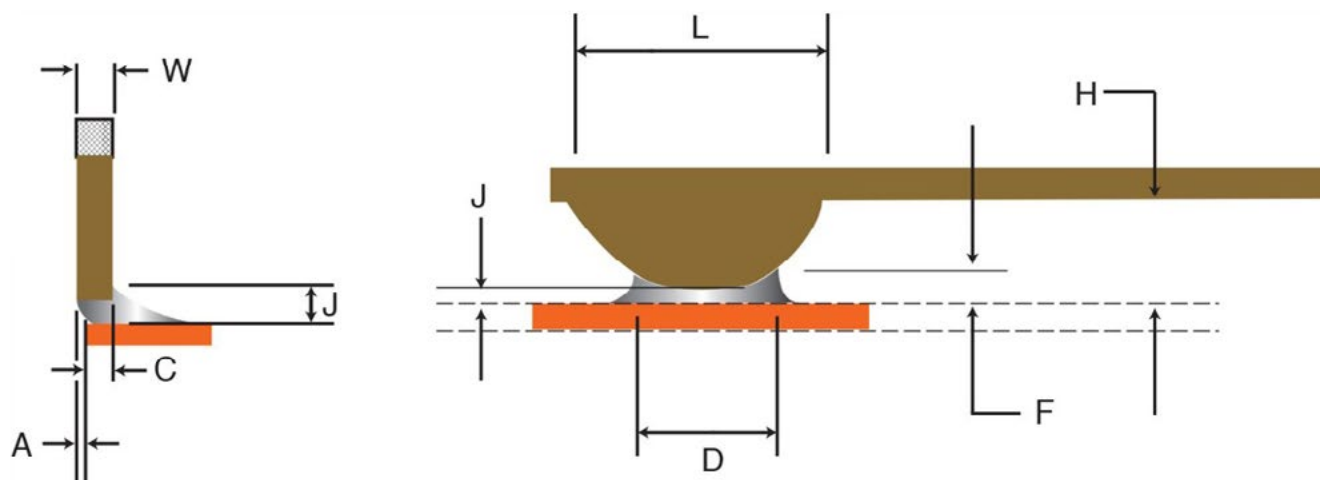
THE PAST, PRESENT, AND FUTURE OF IPC-A-610 *continues*

Figure 1: Example of a P-style connection terminal.

is critical for use during manufacturing. The volunteers developing these two standards often have synergy meetings where they address changes to both documents at the same time.

Specifically for the ongoing development and maintenance of IPC-A-610, it is an industry consensus document prepared by subject matter experts from the electronics industry. The committee consists of more than 200 volunteers representing their companies, organizations, and interests of the industry. It is a truly collaborative project.

On top of that, IPC-A-610 is a global document, readily able to assist electronic assemblies around the world. For example, previous revisions of IPC-A-610 were translated into as many as 20 languages. This expands the reach of the standard, solidifying its usability in the global market. It is all about sharing knowledge and inspiring growth to create a competitive market within the electronics industry.

Latest Revisions

Currently, there are plans to translate the Revision F document. A translation in Chinese is available now, with French, German, and Spanish coming soon. During the F revision efforts, language modifications were made in some instances to ease readability, changes to existing criteria when data showed that a change was needed, and criteria for some new surface mount component types were added.

Some significant changes to IPC-A-610F standard:

- Expanded conformal coating section
- Requirements added for two new SMT terminations
 - P-Style terminations
 - Butt/I terminations—solder charged terminations
- Improved language for ease of readability and understanding
- Revised soldering requirements for plastic SMT components
- New photos added for clarity
- Class 2 plated through-hole vertical solder fill requirements revised
- Simplified Imperial English dimensions utilized in the documents

Training, Certification, and Validation Services

There is currently a training protocol for IPC-A-610F available for those who want to participate in an industry-recognized training and certification program. This training protocol provides Master Trainers (MITs) and Certified Trainers (CITs) the full complement of course materials required for training and certification of individuals at companies within the electronics industry. Individuals are trained and take an exam to be certified on how to use IPC-A-610F in their specific roles within their own companies. This training and certification of employ-

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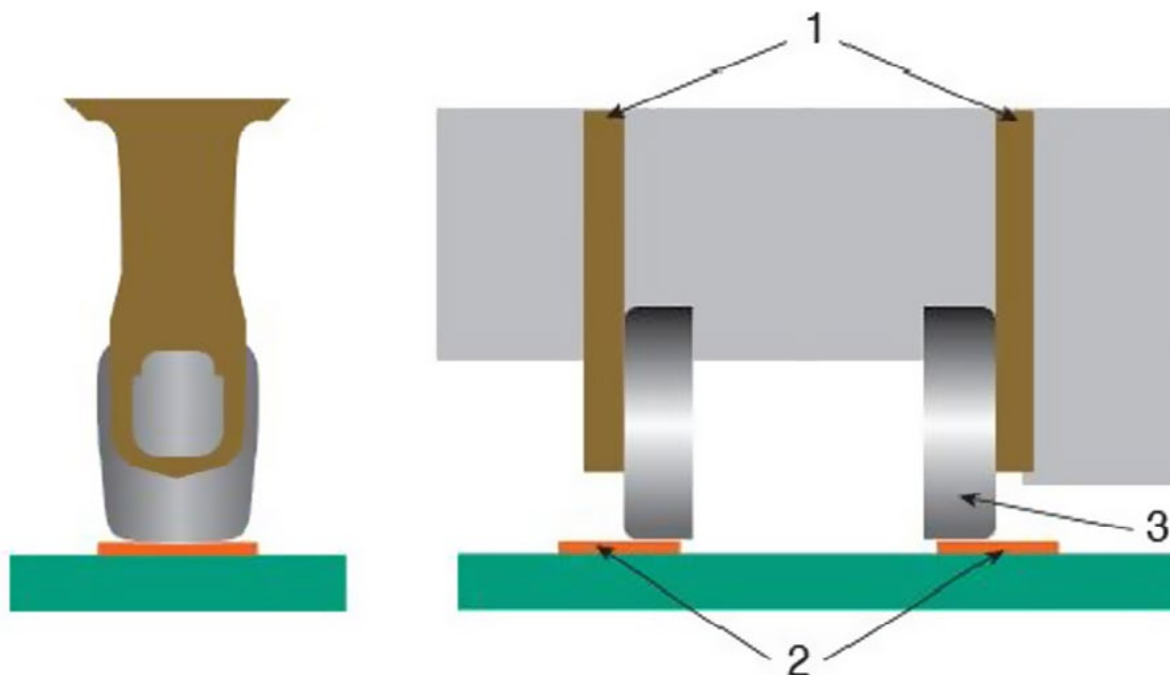


Figure 2: Example of a butt/l connection—solder charged termination.

ees to IPC standards provides the added level of quality performance companies look for in the electronics industry.

IPC has also embarked on a program, Validation Services, to address the certification of a company's manufacturing assembly practices to the IPC-A-610F standard. A Qualified Manufacturers Listing (QML) is an assessment/audit done by IPC of a company's capabilities to meet class 1, 2, or 3 of IPC's standards. The program takes certification to the next level for EMS, ODM, and OEM companies.

A company's quality and success is often depicted in the form of a pyramid. IPC has adapted the pyramid as it applies to standards, training/certification and validation for EMS, ODM and OEM companies. The base of the pyramid is the use of IPC Standards. The next level of value delivered is individuals trained and certified to IPC's standards for their given companies. At the highest level of value delivered is the QML recognition, which certifies the company's manufacturing and quality process. By completing all levels of the IPC pyramid, companies have an opportunity to show their customers and suppliers, they have a complete

quality product as a supplier in the electronics assembly supply chain.

Conclusion

IPC-A-610F is a must-have standard for electronics assemblers worldwide. It is available in numerous languages with more translations planned in the coming months, and many companies use it in conjunction with J-STD-001 and other IPC standards. Where people and processes bring products to life, it is IPC standards that can bring consistent criteria and communication to the electronics community. For information about IPC-A-610F, [click here](#).

IPC continually facilitates the evolution of industry standards, and as the industry moves forward, we anticipate the same for this essential document. **PCBDESIGN**



Teresa Rowe is IPC's director of assembly & standards technology, and staff liaison for IPC-A-610. She has more than 25 years of experience in the electronics industry and standards development activities.

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IPC-A-610: What's New with Rev F?

by **Leo Lambert**

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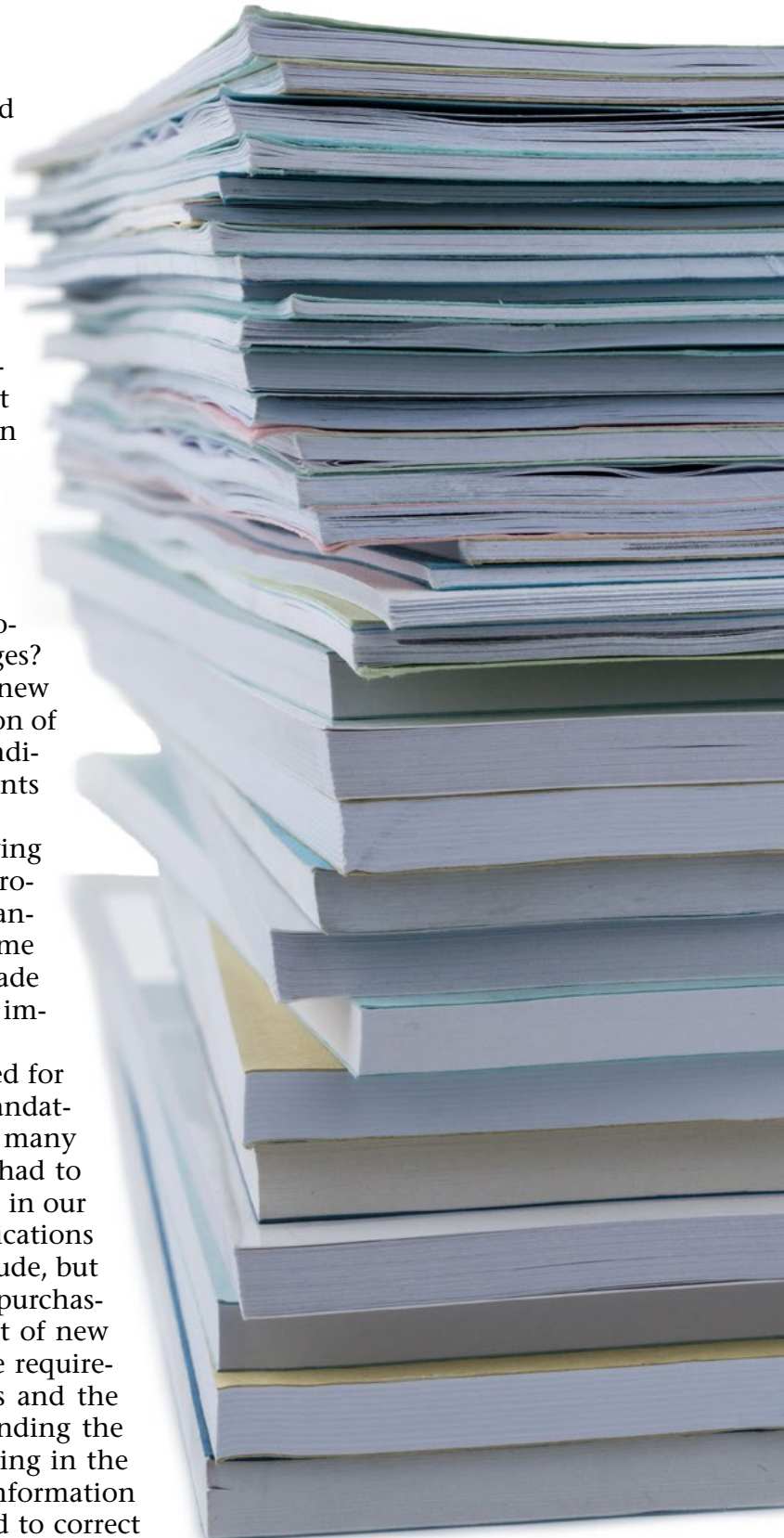
IPC generates many specifications related to printed circuit board fabrication, assembly processes and inspection criteria. The intent of the following article is to describe how the documents come about and how they are generated by providing an overview of the latest changes in IPC-A-610, Acceptability of Electronic Assemblies, hereafter identified as 610. Additionally, there are online courses available that will go through each one of these changes in details.

Background

Why are new revisions created? Can't IPC just issue updates to the existing revision? Who defines what the changes are going to be and who approves of those changes? Why can't they make changes for all the new technologies available? And the best question of all: Why does my product have some conditions that are not covered in the documents and specifications?

Taking just one document, 610, and trying to answer those questions will hopefully provide a window for customers, users, and manufacturers to see where these documents come from and how they are put together to upgrade the products being made, and hopefully improve the quality of those products.

Every five years, a new revision is created for all the specifications from IPC. This was mandated for all ANSI approved documents. Since many IPC documents were ANSI-approved, they had to be reviewed and updated on a regular basis, in our case five years. There are multitudes of implications with the release of new revisions. They include, but are not limited to: contract negotiations, purchasing of new specifications, and development of new certification training programs to cover the requirements of those documents for the trainers and the specialist. This is all accomplished by attending the semiannual meetings of IPC and participating in the task group meetings, where all the new information is presented, all the comments are reviewed to correct

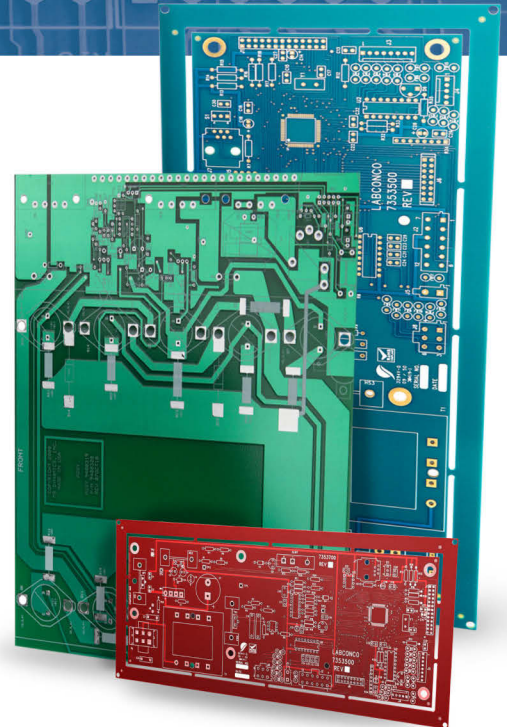


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IPC-A-610: WHAT'S NEW WITH REV F? *continues*

deficiencies in the existing revision, and all conflicting information is reviewed to verify that complementary documents are in agreement for criteria information.

Once all the information is reviewed and accepted by the committee, a draft is sent to the IPC community for review and comment. Once again there is a review and discussion on the comments, and subsequently another draft is created and the process repeats itself until all the comments are resolved and a new document is published.

Creating updates to the documents is also handled in the same fashion, and since the comments are considered critical, the review period is shorten to enhance the speed to which the approval cycle is made and then the documents are published for the user community. This is a relatively short process as it only addresses critical issues to the main body of the document.

So, what defines the changes? First, comments from the user community as found on the comment sheet in the back of every IPC specification. Second, submittal from the component manufacturers on new components being introduced for new technology applications. Finally, corrections needed from editorial and technical mishaps in the existing documents.

Introduction to 610 Changes

The changes from Rev E to Rev F of IPC-A-610 are as follows:

In going through the changes, there are some which reflect not necessarily the inspection of the product but the skills of the operators/inspectors. For example, the first major change is in the scope of the document where we added the statement "...this standard does not provide criteria for cross-section evaluations," as this would be a defect analysis situation and this is

not the intent of the document, because this is an inspection document. Then we added the Personnel Proficiency requirement statement to reflect a synergy issue with the J-STD-001 document. The ESD section was modified to include the information from ANSI/ESD-S-20.20 and other related ESD documents.

Chapter 4 was modified to discuss torque, which is a new inclusion into the document including wire routing, bend radius, and the use of tie wraps.

Chapter 6 discusses the importance of wire stripping and no damage to the insulation and the wire strands. Table 6-10 was modified to try to make the criteria less confusing when using wire that is less than 30 AWG. There were also changes in the Swage Hardware section for the terminal base to land separation, which was included to make sure the terminals were not loose on the boards.

Chapter 7 discussed adhesive bonding of components and how it is acceptable if and when the adhesive goes beneath the component.

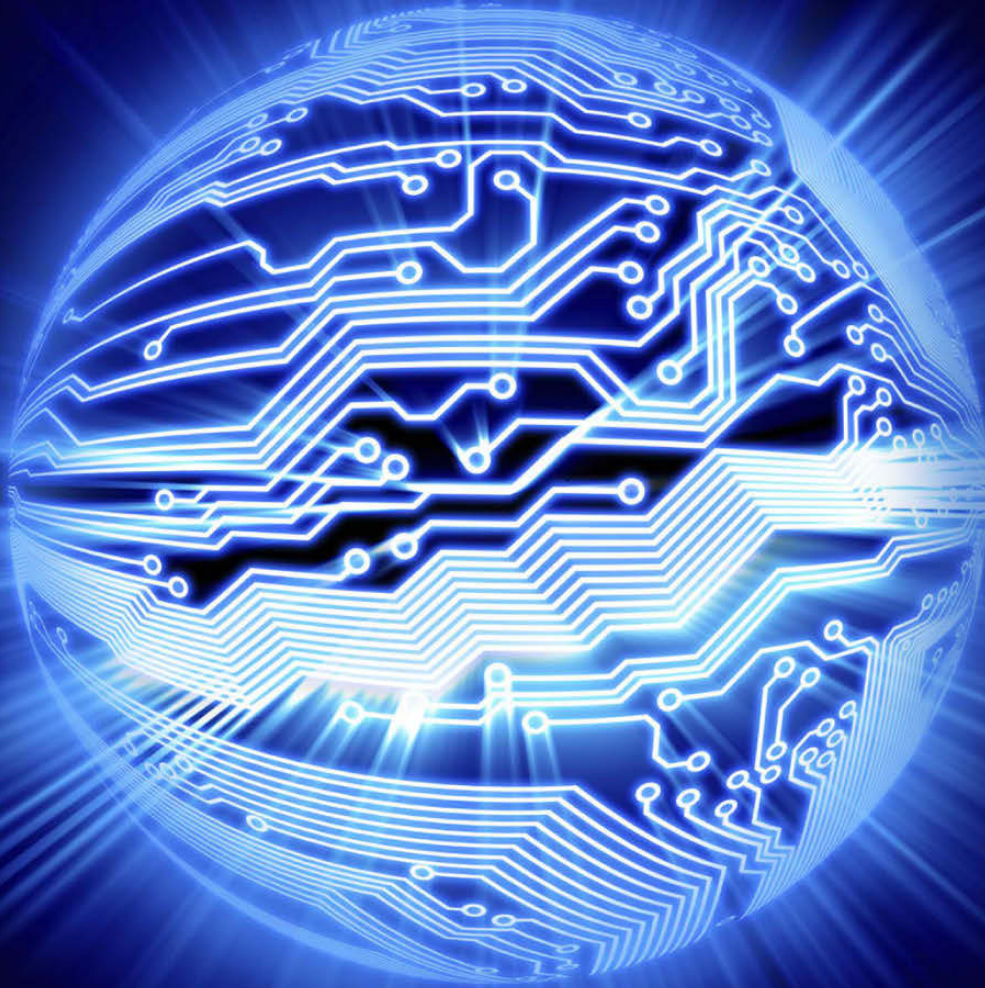
The important section of this chapter is 7.3.5 Supported Holes –

Solder. The criteria for solder fill of the plated through holes with solder for components with more than 14 leads. When this was added to the document, the section for less than 14 leads was left out, and due to that mistake an amendment is being readied for release to correct this issue. If and when this does come up, the recommendation is to continue using the Rev E criteria. In section 7.5.6 Jumper Wires Lap Soldered, it expands on the assembly of those wires to land areas and surface mount components for the type of solder joints which are created when attaching jumper wires to the boards.

Chapter 8 discusses staking adhesives and changes the criteria for coverage of components when applying the adhesive, it also goes into changing the definition of low-profile compo-

“
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IPC-A-610: WHAT'S NEW WITH REV F? *continues*

nents to plastic components where solder is allowed to climb the lead and touch the body of the component. This criteria has been in 610 for at least four revisions, so to make it a little less ambiguous due to the number of new components being introduced it was decided to make a difference between plastic and other body materials being used for the fabrication of components. Additionally, since this is the chapter on surface mount components, there are changes in the Class 3 requirement for chip components to have minimum end overlap expanding on the definition of billboarding and its acceptability for certain size chip components.

There is also the new requirement for the solder charge terminations, which are a butt joint component that is being introduced for use in Class 3 products. Although the debate is still ongoing, this is a new component which may end up being used on Class 3 products. The voiding criteria in BGA balls was changed from 25, to 30%, and it also discusses champagne voids at the board to BGA solder ball interface which will impact product reliability if

not watched carefully. The criterion for bottom thermal plane termination was also expanded to clarify the requirement. Finally the addition of criteria for "P" style terminations, a new component being introduced which is applied by sliding it over the edge of the circuit board and soldering the terminations on both sides of the board.

Section 10 was modified to bring it into line with IPC-A-600, Acceptability of Printed Boards.

If you'd like to get involved with IPC standards such as IPC-A-610, the standards committees always welcome new volunteers. Check the EPTAC [website](#) for more information about IPC-A-610 and related training. **PCBDESIGN**



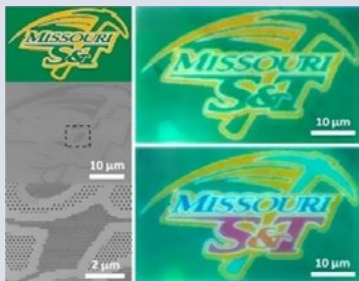
Leo Lambert is vice president and technical director of the training company EPTAC Corporation.

"No-ink" Color Printing with Nanomaterials

Researchers at Missouri University of Science and Technology are giving new meaning to the term "read the fine print" with their demonstration of a color printing process using nanomaterials.

The researchers describe their "no-ink" printing method in the latest issue of the journal [Scientific Reports](#) and illustrate their technique by reproducing the Missouri S&T athletic logo on a nanometer-scale surface.

The researchers' printing surface consists of a sandwich-like structure made up of two thin films of silver separated by a "spacer" film of silica. The top layer of silver film is 25 nanometers thick and is punctured with tiny holes created by a micro-



fabrication process known as focused ion beam milling.

The researchers created a scaled-down template of the athletic logo and drilled out tiny perforations on the top layer of the metamaterial structure. Under a scanning electron microscope, the template looks like a needlepoint pattern of the logo. The researchers then beamed light through the holes to create the logo using no ink – only the interaction of the materials and light. This allowed researchers to create different colors in the reflected light and thereby accurately reproduce the S&T athletic logo with nanoscale color palettes.

"Unlike the printing process of an inkjet or laserjet printer, where mixed color pigments are used, there is no color ink used in our structural printing process – only different hole sizes on a thin metallic layer," says Dr. Jie Gao, an assistant professor of mechanical and aerospace engineering at Missouri S&T and a co-author of the paper.



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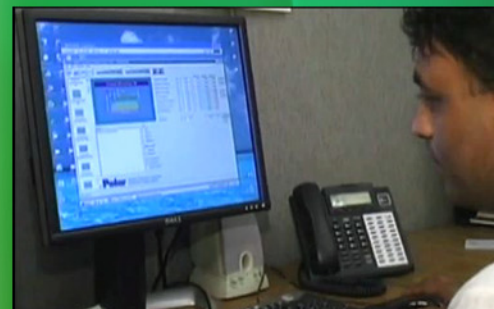
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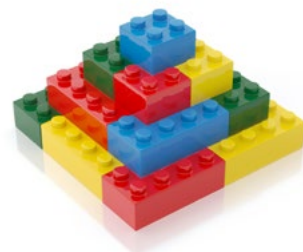
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Stackup Planning, Part 1

by Barry Olney

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The PCB substrate that physically supports the components, links them together via high-speed interconnects and also distributes high-current power to the ICs is the most critical component of the electronics assembly. The PCB is so fundamental that we often forget that it is a component and like all components, it must be selected based on specifications in order to achieve the best possible performance of the product. Stackup planning involves careful selection of materials and transmission line parameters to avoid impedance discontinuities, unintentional signal coupling and excessive electromagnetic emissions.

The complexity of electronics design is undoubtedly going to increase in the future, presenting a new set of challenges for PCB designers. Materials used for the fabrication of multilayer PCBs absorb high frequencies and

reduce edge rates, thus putting the materials selection process under tighter scrutiny. Ensuring that your board stackup and impedances are correctly configured is a good basis for stable performance.

So where do we start? Over the years, I have found that many engineers and PCB designers do not understand the basic structure that makes up a substrate. We all know that multilayer PCBs consist of signal and plane layers, dielectric material and soldermask coating, but there is a lot more to it.

The most popular dielectric material is FR-4 and may be in the form of core or prepreg (pre-impregnated) material. The core material is thin dielectric (cured fiberglass epoxy resin) with copper foil bonded to one or both sides. For instance: Isola's FR406 materials include 5, 8, 9.5, 14, 18, 21, 28, 35, 39, 47, 59 and 93 mil

ICD Stackup Planner | Field Solver Technology

File Edit Export Import Setup Help

Stackup Planner PDN Planner

2 Layer 4 Layer 6 Layer 8 Layer 10 Layer 12 Layer 14 Layer 16 Layer 18 Layer New 8 Layer

UNITS: mil 9/17/2014 Total Board Thickness: 63 mil

Differential Pairs > 50/100 USB DDR3

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Z0)	Edge Coupled Differential (Zdiff)	Broadside Differer
		Soldermask		Liquid Photoimageable	3.8	0.5							
1	8 4 8	Signal	Top	Conductive			2.2	8	4	0.43	53.5	98.11	
		Prepreg		370HR; 1080; Rc= 66% (5GHz)	3.72	2.9							
2		Plane	GND	Conductive			0.7						
		Core		370HR; 1-1652; Rc=43% (5GHz)	4.2	5							
3		Signal	Inner 3	Conductive			0.7	8	4	0.19	54.03	101.32	
		Prepreg		370HR; 7628; Rc= 50% (5GHz)	4.05	8							
4		Plane	VDD	Conductive			0.7						
		Core		370HR; 3-7628/1080; Rc=44% (5G...	4.2	24							
5		Plane	VSS	Conductive			0.7						
		Prepreg		370HR; 7628; Rc= 50% (5GHz)	4.05	8							
6		Signal	Inner 6	Conductive			0.7	8	4	0.19	54.03	101.32	
		Core		370HR; 1-1652; Rc=43% (5GHz)	4.2	5							
7		Plane	GND2	Conductive			0.7						
		Prepreg		370HR; 1080; Rc= 66% (5GHz)	3.72	2.9							
8		Signal	Bottom	Conductive			2.2	8	4	0.43	53.5	98.11	
		Soldermask		Liquid Photoimageable	3.8	0.5							

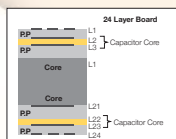
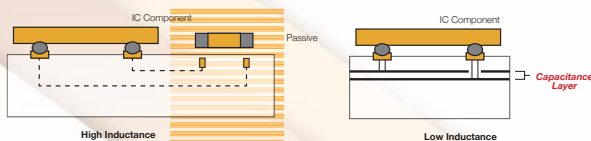
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Figure 1: A typical 8-layer PCB stackup used for high-speed design.

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STACKUP PLANNING, PART 1 *continues*

cores. The copper thickness is typically 1/3 to 2 oz. (17 to 70 μm).

The prepreg (B-stage) material is comprised of thin sheets of fiberglass impregnated with uncured epoxy resin which hardens, when heated and pressed, during the PCB fabrication process. Isola's FR406 materials include 1.7, 2.3, 3.9 and 7.1 mil prepregs that may be combined to achieve thicker prepreg.

The most common stackup is called the foil method. This features prepreg with copper foils bonded to the exterior on the outermost layers (top and bottom). Core then alternates with prepreg throughout the substrate. An alternate stackup is known as the capped method, which is the opposite of the foil method and was used by old-school military contractors.

FR-4 has industry approvals of IPC-4101B and is Underwriter Laboratories (UL) recognized for product safety. FR-4 has a glass transition temperature (T_g) of 170°C (the temperature at which the resin begins to flow and the substrate changes to a viscous

state) and a decomposition temperature (T_d) of 294°C (the temperature at which the substrate breaks down or decomposes). The peak reflow temperature for lead-free solder is 260°C, which is only held for 20 seconds, to reflow solder the surface mount components to the substrate. RF-4 can be used for designs up to 1 GHz.

The Rogers materials (RO4350 & RO4003) are another common dielectric that can withstand higher temperatures ($T_g > 280^\circ\text{C}$ and $T_d = 425^\circ\text{C}$), and they are ideal for high-speed designs up to 10 GHz. But this is somewhat more expensive than FR-4.

The total substrate thickness is generally 62 mil (1.6 mm), but may vary according to the application: 20, 31, 40, 47, 62, 93 and 125 mil are a few other not-so-typical thicknesses. Backplanes, for instance, will typically use the thicker substrate to ensure mechanical support.

One of the steps of the PCB fabrication process is lamination. Core materials are pinned together in a lamination book with sheets of prepreg separating copper layers. The prepreg basically glues the core materials together. Outer layers are made of a foil of copper, which is etched last in the process, so the outer layers of prepreg act as cured core. Horizontal alignment is critical. The stack is pinned between two heavy metal plates and put in a heated hydraulic press for about two hours, until cured.

In Figure 3, the left stackup has a total thickness of 9 mil. However, when the board is cured the resin in the prepreg (green) flows around the signal traces below (as in the right diagram). This envelopes the trace completely, and also thins the prepreg material. As the signal trace becomes closer to the above plane, the impedance drops.

So, here are a few effects of the prepreg being cured:

a) The total board thickness reduces, by the thickness of the signal layer copper, as the trace is totally enveloped in resin from the prepreg. The resin also flows into the antipads of the nearby planes and oozes from the sides of the lamination book.

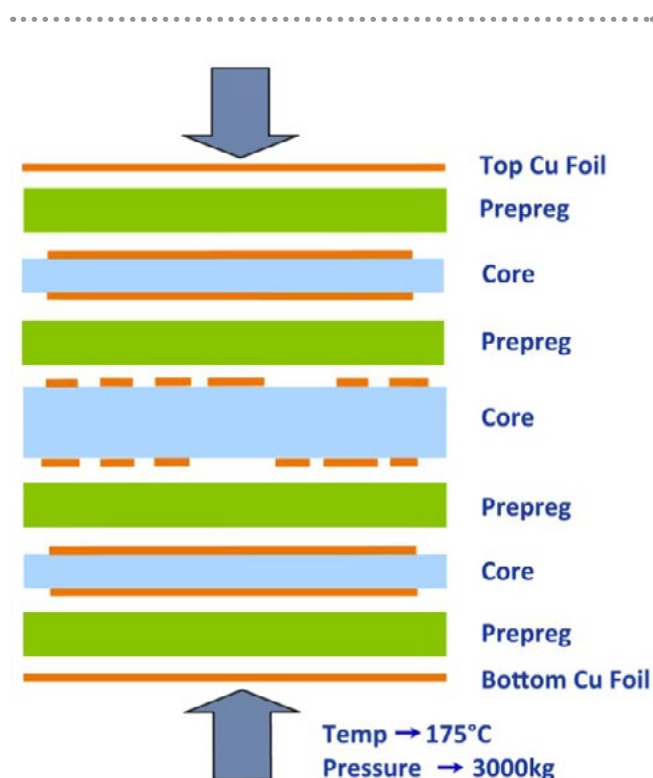
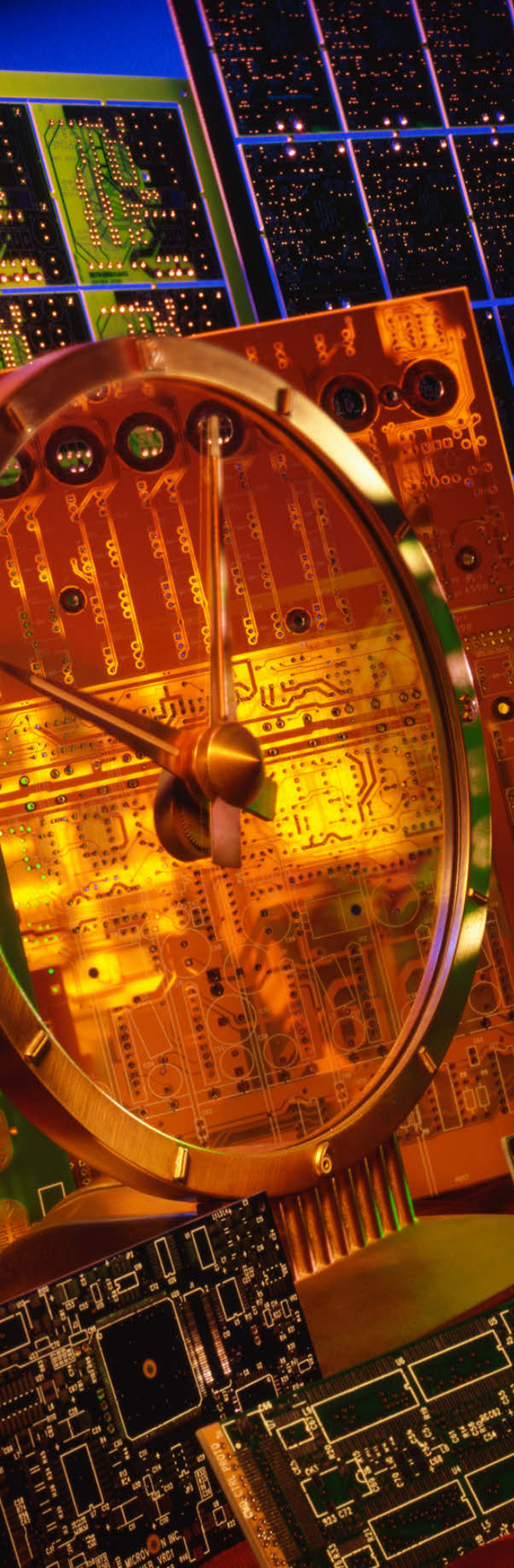


Figure 2: The PCB lamination process.



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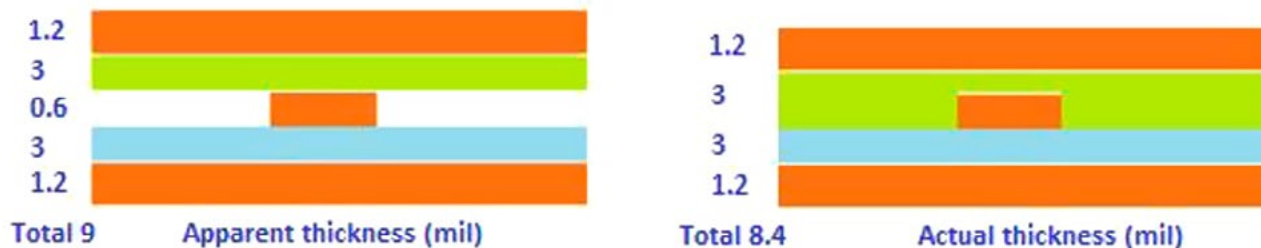
STACKUP PLANNING, PART 1 *continues*

Figure 3: Total board thickness.

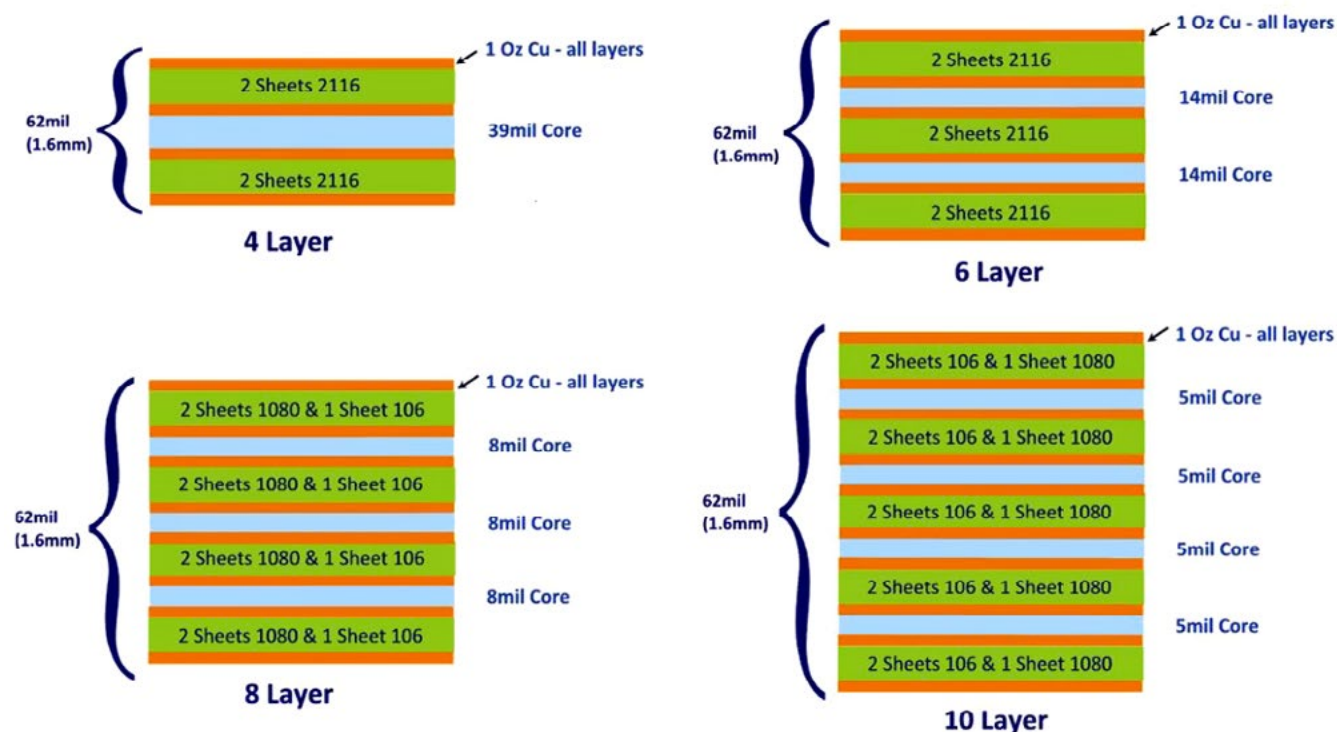


Figure 4: Typical stackups. (source: Advanced Circuits)

b) The impedance of the signal trace reduces as the resin flows out of the prepreg around the traces and makes the prepreg thinner. This results in the trace becoming closer to the plane.

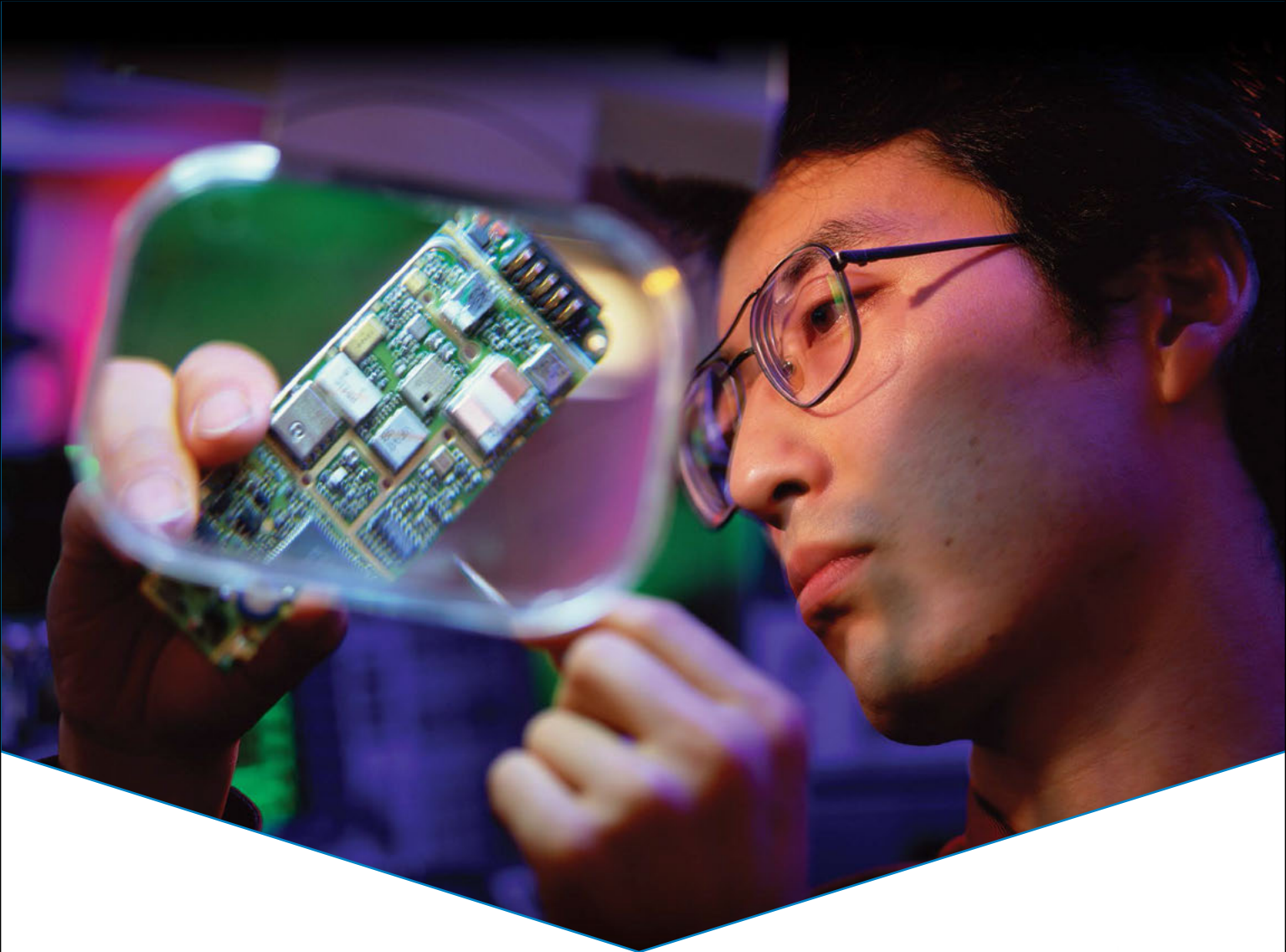
c) The edge of the PCB can have less resin than the centre (and therefore slightly different impedance) due to resin flowing out of the edge of the lamination book. The resin/glass percentage, across the entire panel, determines the impedance—the more resin the higher the impedance.

d) Buildup layers—the outer most prepreg and copper—are etched last in the fabrication process so the resin does not flow around the outer layer copper traces. In this case, the trace thickness is added to the total board thickness and the impedance does not change.

The stackups of Figure 4 are typical stackups for 62 mil substrates, although they may vary between PCB fabricators as they may stock different materials.

Please note the following:

- The outermost dielectric is prepreg.



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STACKUP PLANNING, PART 1 *continues*

- The outer prepreg has a copper foil coating.
- Prepreg layers may be combined with (multiple) sheets of prepreg separating them. For instance, two sheets of 1080 and one sheet of 106 prepreg material may be required to achieve the desired thickness.

So where do we start in an attempt to build the perfect stackup for our project? Initially, virtual materials are used to get the rough numbers. Obviously, every digital board will require 50 ohms impedance and generally a 100 ohm differential pair. This is our target impedance. However, multiple technologies are often used on complex designs.

Keep these tips in mind when planning the board stackup:

- All signal layers should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies. Closely coupled planes reduce AC impedance at the top end and dramatically reduce electromagnetic radiation.
- High-speed signals should be routed between the planes to reduce radiation.
- Reducing the dielectric height will result in a large reduction in your crosstalk without having a negative impact on available space on your board.
- The substrate should accommodate a number of different technologies. For example: 50/100 ohm digital, 40/80 ohm DDR4, 90 ohm USB.

Unfortunately, not all of these rules can be accommodated on a four-layer or six-layer board simply because we have to use a buffer core in the center to realize the total board thickness of 62 mil. However, as the layer count increases, these rules become more critical and should be adhered to.

Part 2 of the Stackup Planning series will continue detailing the construction of typical, high layer-count stackups and build-up technology.

Points to Remember

- The PCB substrate is the most critical component of the electronics assembly.
- Ensuring that your board stackup and impedances are correctly configured is a good basis for stable performance.
- Dielectric material may be in the form of core or prepreg (pre-impregnated) material. The core material is thin dielectric (cured fiberglass epoxy resin) with copper foil bonded to one or both sides. The prepreg material is thin sheets of fiberglass impregnated with uncured epoxy resin which hardens when heated and pressed.
- The total substrate thickness is generally 62 mil (1.6 mm) but may vary according to the application.
- When the board is cured, the resin in the prepreg flows around the signal traces below, thus enveloping the trace completely and also thinning the prepreg material. This alters the impedance of the signal traces.
- To construct a stackup: Initially, virtual materials are used to get the rough numbers then exact materials from the library are introduced to improve accuracy. **PCBDESIGN**

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2. Henry Ott: Electromagnetic Compatibility Engineering.
3. Bob Tarzwell: Controlled Impedance.
4. The ICD Stackup and PDN Planner: www.icd.com.au.



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, [click here](#).



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A Conversation (and Day) with Joe Fjelstad

I-Connect007 Publisher Barry Matties and industry veteran Joe Fjelstad, CEO and founder of Verdant Electronics, recently spent a day together enjoying the Oregon community of McMinnville (home of the Spruce Goose), where their conversation ebbed and flowed between a wide variety of topics. The result is this five-part interview series that covers a lot of ground, from the war on process failure and the future of the electronics industry, to political shenanigans, the direction of lead-free, and more.

Design Considerations: Flexible Circuit vs. Traditional PCB

The tactics for flexible circuit design don't differ much from that of traditional PCBs. All of the typical specifications still apply and we add a few more things that require special attention. Cover layers require bigger openings than traditional solder mask, trace directions matter in the flex areas and miters should be round instead of angular.

Impact 2015: An In-Depth Look

IPC understands that presenting a unified voice for the electronics industry is essential for advancing policies that affect the industry's long-term future and strengthens the U.S. and global economy. That is why 22 IPC member-company executives descended on the nation's capital for IMPACT 2015: IPC on Capitol Hill, IPC's annual advocacy event.

AT&S Boosts Investments in Chongqing China Plant

AT&S is one of the globally leading manufacturers of high-end HDI and any-layer printed circuit boards. Key trends in this industry include the ongoing miniaturisation and increasing modularisation.

German PCB Sales Up 2.6% in March

March PCB sales in Germany went up by 2.6% compared to the same period last year, mainly driven by the industrial electronics sector, according to ZVEI PCB and Electronic Systems.

U.S. Circuit Celebrates 30 Years of PCB Fabrication

President Mike Fariba has built U.S. Circuit into a successful business through his guiding principles of hiring the best people, providing the customer with high quality products and service, and using the latest leading edge technology, all with a commitment to continuous improvement.

PCB Industry to Achieve CAGR of 4% over 2015-2020

The major drivers of the PCBs market are growing demand for 3C applications (communication, computer/peripheral, and consumer electronics), advancement in PCB technologies, and increased demand of aerospace and defense products.

AT&S Hits Record Revenues in Preliminary Results 2014/15

"We saw a disproportionately high benefit from the strong growth in the area of mobile devices, especially smartphones, and from the constantly increasing share of electronics in the automotive sector throughout the year. This led to the highest revenue in the company's history to date," says Andreas Gerstenmayer, chairman of the management board of AT&S AG.

TTM Posts Q1 Results, Sees Benefits from Acquisition of Viasystems

"We are pleased to report strong operating results in the first quarter, with revenue at the high end and non-GAAP earnings above our initial guidance ranges," said Tom Edman, CEO of TTM. "Viasystems will bring TTM meaningful strength in the automotive end market and will complement our position in other end markets, enabling us to continue to broaden our product portfolio to address an increasingly diverse set of end markets."

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Avoiding Overload in Gain-Phase Measurements

by Istvan Novak
ORACLE



Today, most of our printed circuit boards have at least a few DC-DC converters, and some boards have many. We have a large choice when it comes to deciding what to use: we can design and build our own converter from discrete parts (called voltage regulator down or VRD) or we can buy one of the off-the-shelf open-frame or fully encapsulated voltage regulator modules (VRM). For low currents we can use linear regulators; for medium and high current we are better off using a switching-mode topology. Whatever circuit

best suits our needs, chances are that we want to keep the output voltage regulated against changes in input voltage and load current, which in turn calls for one or more internal control loops.

There is a well-established theory to design stable control loops, but in case of power converters, we face a significant challenge: Each application may require a different set of output capacitors coming with our loads. Since the regulation feedback loop goes through our bypass capacitors (shown as a single C_{out}

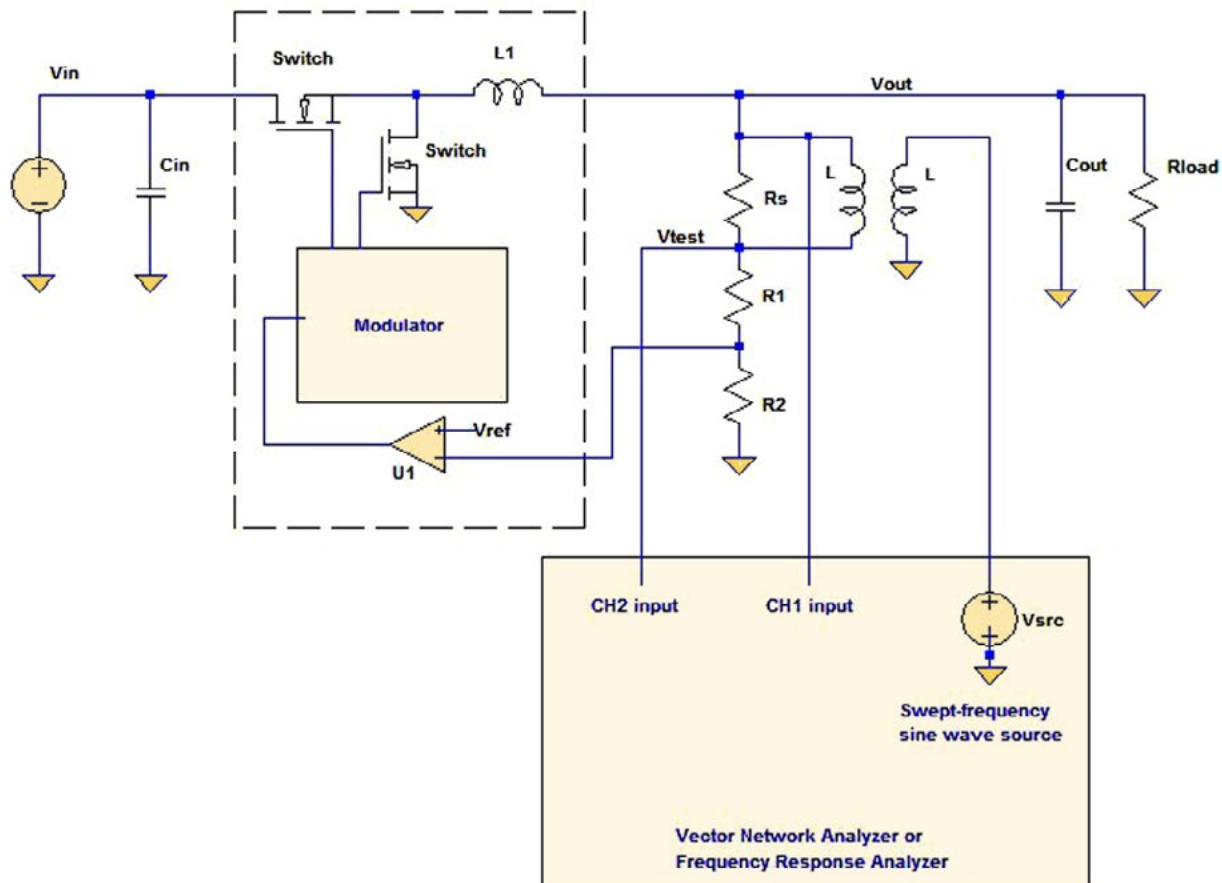


Figure 1: Block diagram of a typical DC-DC converter and gain-phase test setup.

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AVOIDING OVERLOAD IN GAIN-PHASE MEASUREMENTS *continues*

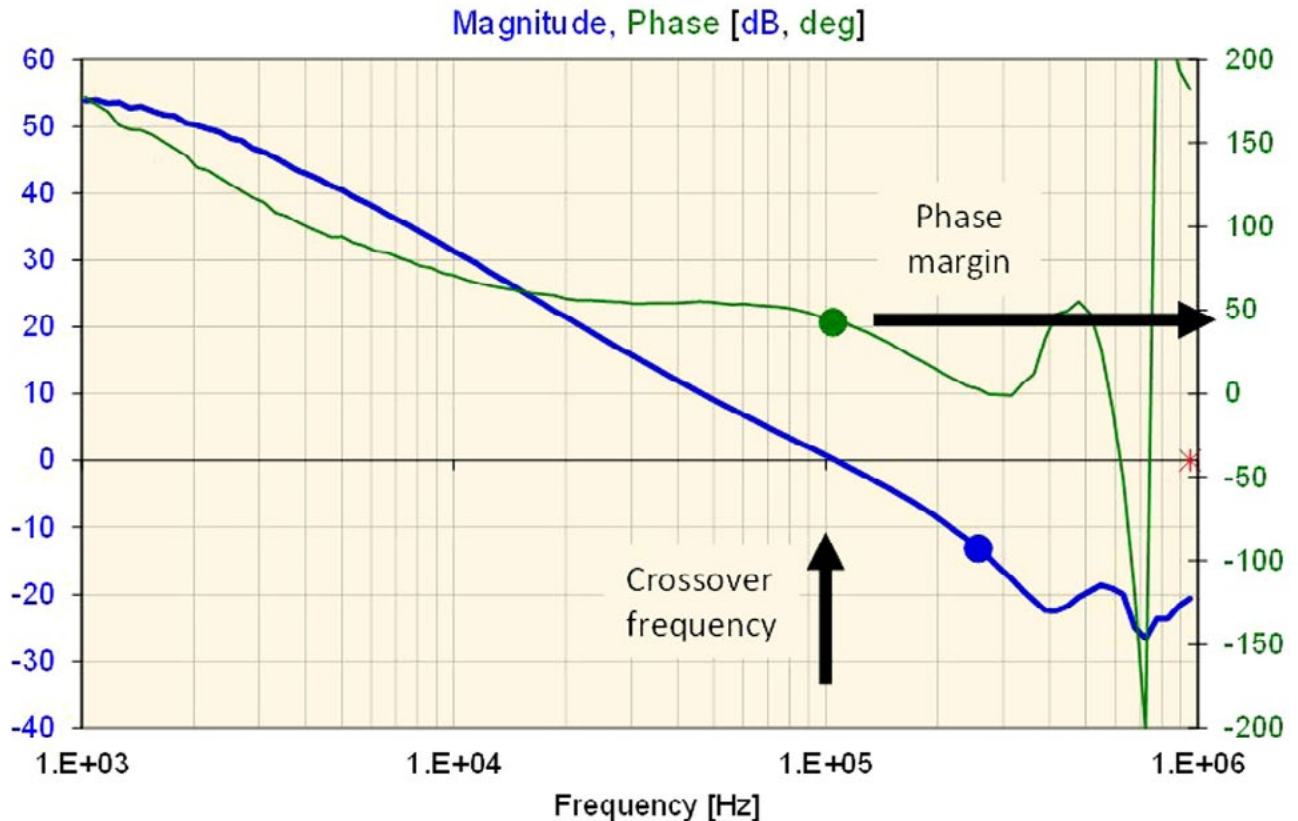


Figure 2: Typical gain-phase plot with the phase margin identified.

in Figure 1), our application-dependent set of capacitors now becomes part of the control feedback loop. Unfortunately, certain combination of output capacitors may cause the converter to become unstable, something we want to avoid. This raises the need to test, measure and/or simulate the control-loop stability.

Figure 1 shows the block diagram of a switching-mode step-down DC-DC converter (also commonly called a buck converter) together with the usual connections and setup for measuring the loop stability. This is also called the gain-phase measurement, because we are mostly interested in the phase of the loop gain as a function of frequency. The phase value where the gain magnitude drops to unity is called the phase margin. A typical measured data set is shown in Figure 2, where the labels identify the phase margin.

The heavy blue line on the chart goes with

the left vertical axis and it shows the loop gain magnitude in dB. The gain magnitude reaches unity (zero dB) at slightly above 100 kHz. There is a large dot at this frequency on the thin green curve, indicating the crossover frequency on the horizontal axis and the phase margin on the right vertical axis. The phase margin in this case is around 45 degrees, which is usually considered as acceptable.

To measure the phase margin, we need to inject a test signal into the control loop. A suitable location is the top of the feedback voltage divider, where it connects to the output voltage. We cut the loop open at this point and insert the test signal in series to the voltage divider. The top side of the signal injection faces the converter output, which is low impedance, whereas the low side of the injection impedance faces the upper voltage divider resistor, which is usually in the hundreds of ohms range or higher.

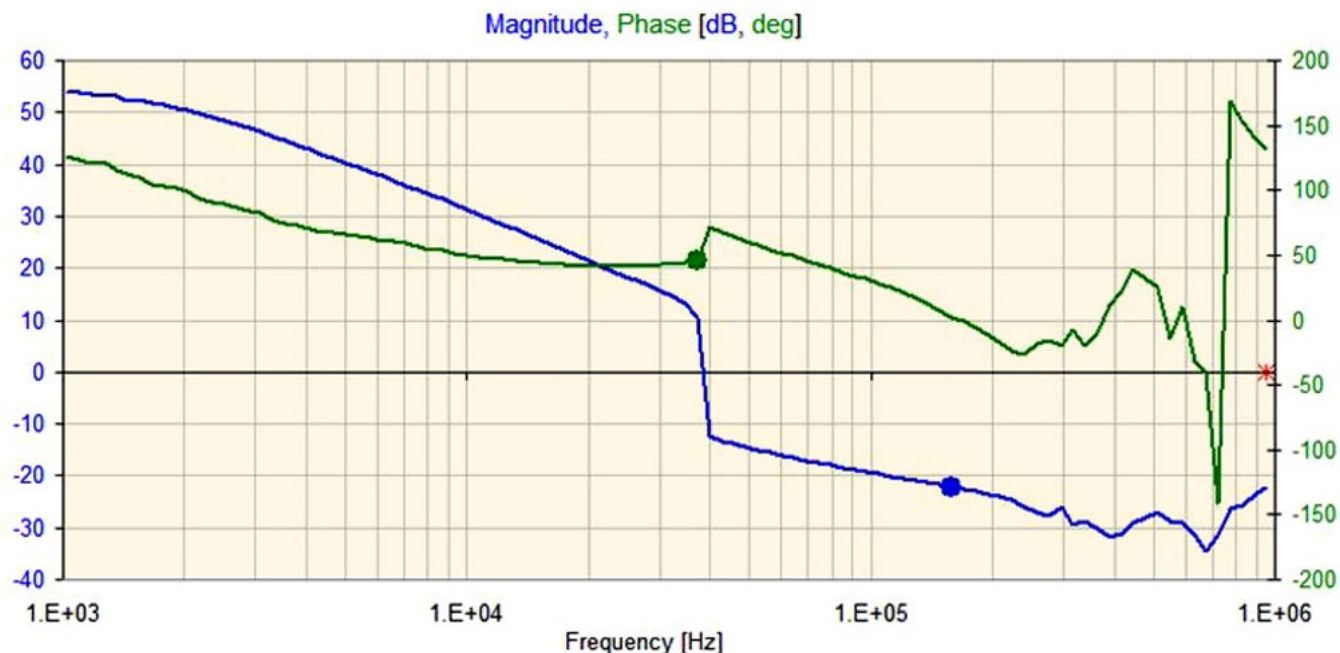


Figure 3: An example of gain-phase plot showing the result of error-amplifier overloading.

Inserting the test signal at such a location guarantees the lowest possible alteration of loop characteristics by the measurement. Since the injection point sits at the DC output voltage, we need an isolation transformer as shown in Figure 1. We can measure the loop gain as the complex ratio of the voltages at the two sides of the injection transformer with respect to ground. There are dedicated instruments for this purpose, called frequency response analyzers.

There is one remaining challenge though, which leads us to the title of this article. As you can see on the chart, the loop gain can vary by orders of magnitudes as frequency changes; usually it is in the 40–70 dB range at very low frequencies. Unless the converter is our discrete component design, we may not know exactly what circuitry we have along the control loop, so it may be hard to guess the proper level of the test signal. If we are not careful and use too large a test signal, we can easily overload the control loop. This in turn will create invalid results. An illustration of such a case is shown in Figure 3.

If, on the other hand, we preemptively try to select a very low injected test signal level, our output data may be buried under noise.

How to maintain the proper injected level to be above the noise floor, yet avoid control-loop saturation, will be explained in a future column. **PCBDESIGN**

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1. [Dynamic Characterization of DC-DC Converters](#), DesignCon 2012, Santa Clara, CA, January 30–February 2, 2012.



Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of “Frequency-Domain Characterization of Power Distribution Networks.” To read past columns, or to contact Novak, [click here](#).

The Art of Bending and Forming PCBs

by John Coonrod

ROGERS CORPORATION

Flexible circuits are designed to be bendable, but bending rigid PCBs is a little unusual. However, many applications that do not use flex circuit technology will also require bending and forming the circuit. Some of these applications use high-frequency circuit materials to create a circuit in a form that enables improved antenna functionality. Another application involves wrapping a circuit around a structure, which sometimes functions as an antenna as well.

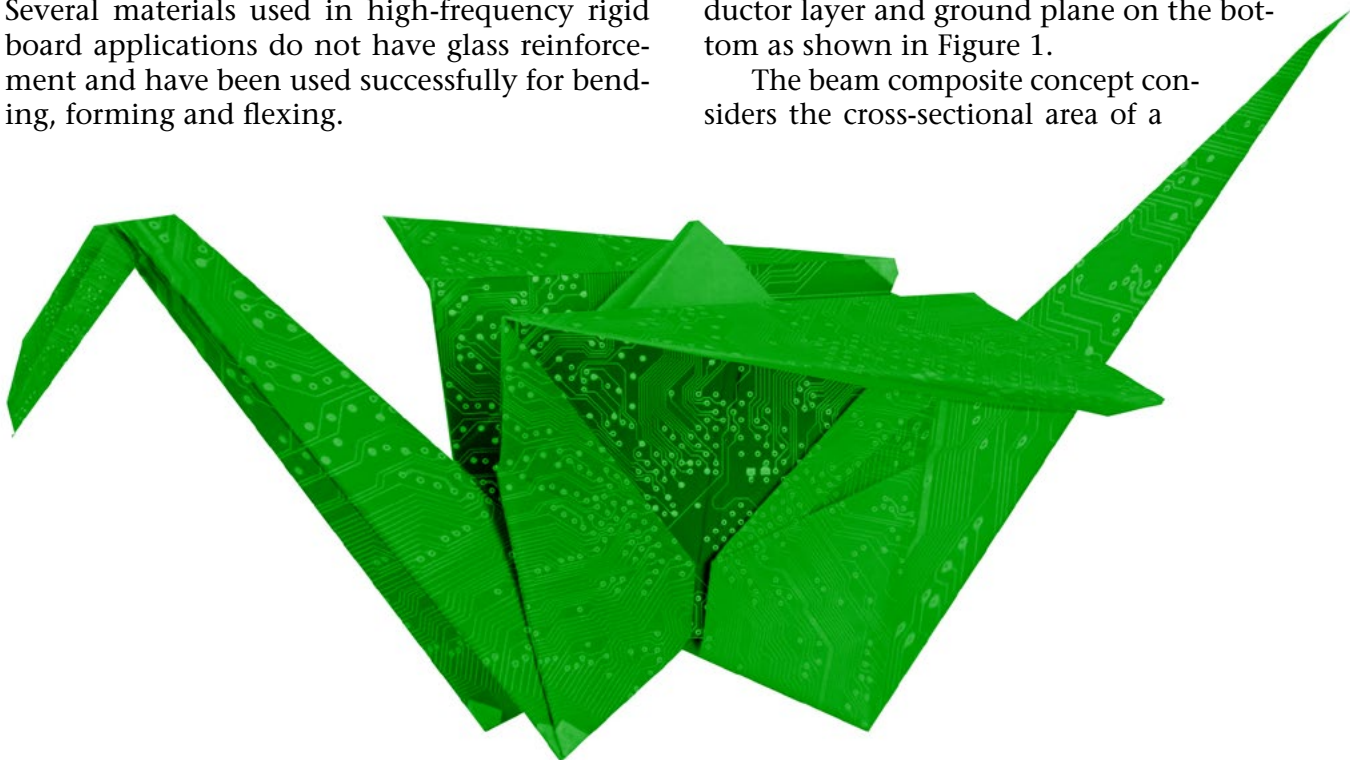
Bending and forming a circuit with dynamic flexing action will require understanding a few basic principles, regardless of the circuit material used. Of course, the circuit material used can make a huge difference in the success of forming circuits without causing conductor or material fracturing. As a general statement with a few exceptions, a circuit material used for bending, forming and flexing cannot have woven glass reinforcement. Because of this, typical FR-4 materials with woven glass are not recommended. Several materials used in high-frequency rigid board applications do not have glass reinforcement and have been used successfully for bending, forming and flexing.

LCP circuit materials are quite suitable for applications where bending, forming and flexing is necessary, and they offer very good high-frequency electrical performance as well. These materials are made as relatively thin laminates, typically less than 5 mils. This thinness aids in the successful bending of the circuits.

However, another set of high-frequency materials has been on the market for many years and used in forming applications: PTFE-based laminates, without glass reinforcement. These materials typically use fillers with the PTFE substrate to help lower the high CTE of PTFE, and this does not detract from the material's bending capabilities.

The basic idea of bending circuits is based on mechanical beam composite theory. As an example, a simple double-sided circuit will be used to demonstrate the concepts. This circuit will be considered a microstrip transmission line with a signal conductor on the top conductor layer and ground plane on the bottom as shown in Figure 1.

The beam composite concept considers the cross-sectional area of a

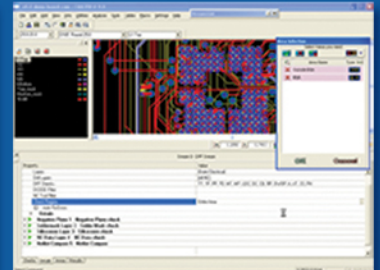
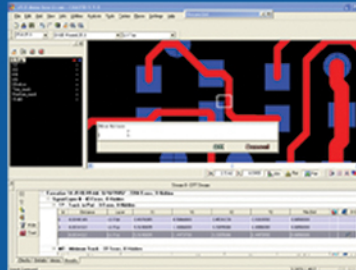


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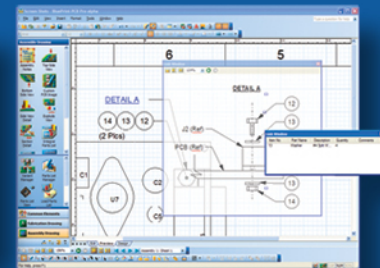
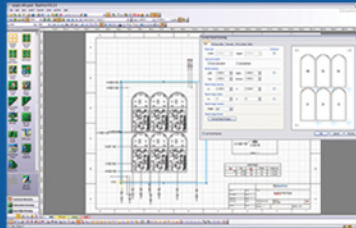
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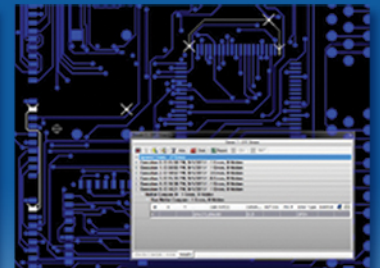
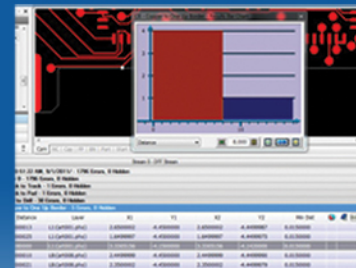
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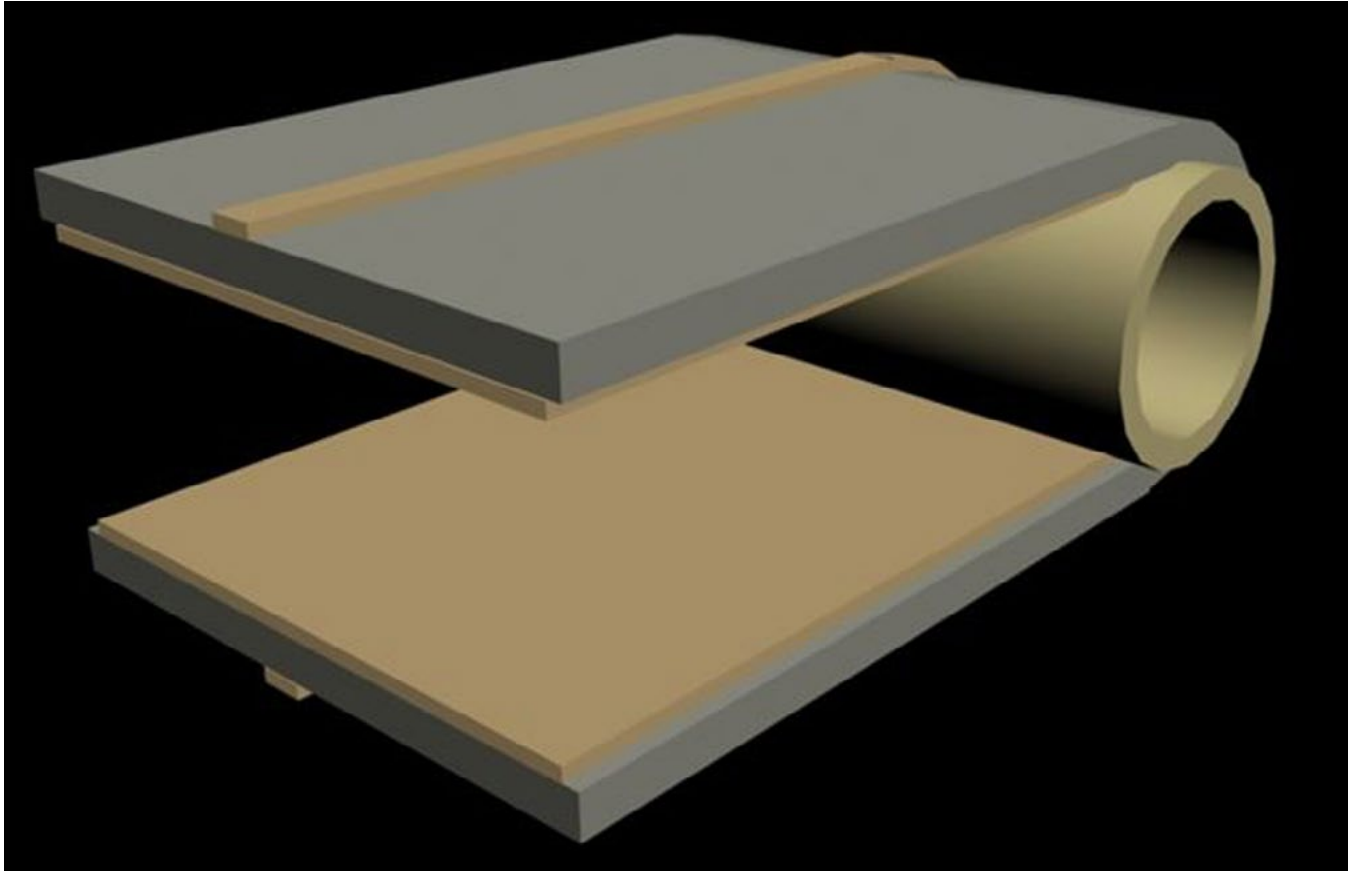
THE ART OF BENDING AND FORMING PCBS *continues*

Figure 1: Double-sided PCB used to demonstrate mechanical beam composite theory.

circuit that is made from different layers of materials. One property critical to understanding bending is modulus; in this case, modulus is the measurement of how stiff the circuit is. A high modulus is stiff, and low modulus is soft. When bending a circuit, softer material will generate less stress within the circuit and when there is less stress, the different layers are less likely to fracture.

Bend radius is another very important issue. A simple way to think about this: If it is necessary to bend a metal sheet that is 1/8" thick without fracturing the metal, then having a large bend radius will be advantageous and, of course, a small, tight bend radius is more likely to cause metal fracturing. The small bend radius causes more internal stress on the metal and is prone to fracturing.

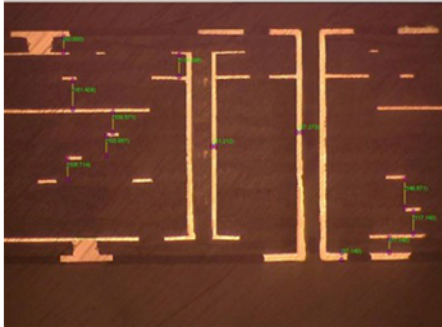
Another concept to consider is the neutral axis of the composite beam (or the circuit). The neutral axis is the plane within the circuit with no stress. Consider bending the 1/8" metal sheet

again and try to imagine the stresses at different thicknesses within the metal sheet. First, the metal at the inside of the bend radius and those layers of the metal sheet will try to compress and will thus have stress due to compression. Then, consider the outside layers of the metal sheet; those layers of metal will try to rip apart or will suffer stress due to tension. Somewhere in the bend area, there is a transition in the metal, from stress as compression to stress as tension. That small transition area that has no stress is called the neutral axis. Ideally, when a circuit is formed, if there is a conductor on the neutral axis it would not fracture, even considering a circuit with a very tight bend radius, because there would be no stress within the conductor.

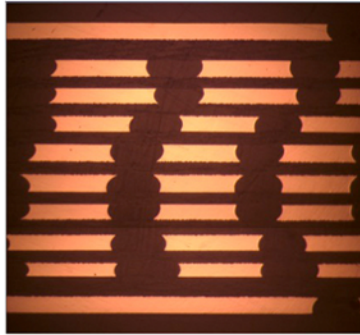
The neutral axis is usually considered while modeling bending, forming and flexing circuits; the idea is to keep the critical copper layers as close to the neutral axis as possible. In the case of the microstrip circuit shown in Figure 1, the neu-

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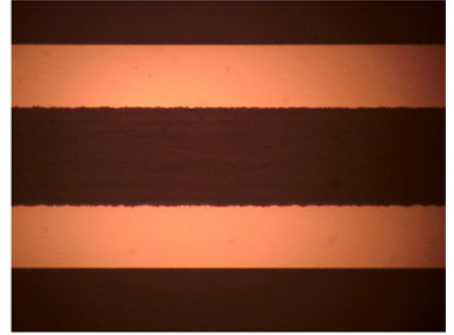
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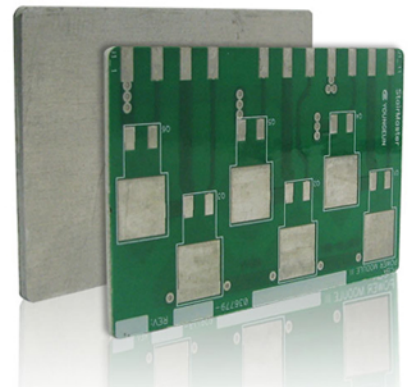
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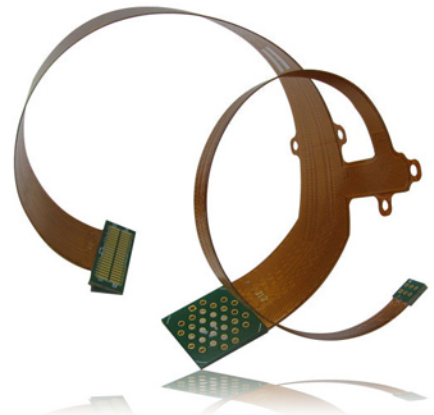
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THE ART OF BENDING AND FORMING PCBS *continues*

tral axis will be located somewhere between the ground plane and the signal plane. That means there will be stress as compression on the ground plane and stress as tension on the signal plane. If a different structure is considered, such as a three-layer stripline circuit with a copper layering scheme of ground-signal-ground, then the neutral axis can be very close to the signal conductor layer. The top and bottom ground layers will have stress as tension and compression respectively, but the signal layer in the geometric center of the cross-section may have very little or no stress. Due to this, the stripline circuit may be formed effectively without damage to the inner signal conductor; however, it is likely to cause some damage on the outer ground plane layers. A thin stripline circuit would minimize the stress on the outer layers and minimize the risk of fracturing.

There are many fabrication variables to consider as well. One is that nickel is very brittle and can easily initiate cracking of the conductor layers. Another issue is copper plating over the laminate copper, which has a potential to have a

copper grain boundary difference and may be an issue for cracking when the circuit is bent. Plated through-holes in the bending area are problematic and the type of copper used on the laminate can be critical.

If more information on bending, forming and flexing of rigid circuits is required, it is best to discuss these issues with your material supplier, or contact a technologist familiar with flexible circuit technology. Many times, bending, forming and flexing a high-frequency circuit board will follow the same basic principles of flexible circuit technology. Even though the two technologies differ electrically, the mechanical aspects are similar. **PCBDDESIGN**



John Coonrod is a senior market development engineer for Rogers Corporation. To read past columns, or to reach Coonrod, [click here](#).

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Stretchable Inks: Changing the Wearables Market and the Landscape of Manufacturing

I-Connect007 Publisher Barry Matties and DuPont's Steven Willoughby and Michael Burrows spoke recently and discussed a new material for wearable electronics: stretchable inks. Wearable electronics is a fast growing sector of the electronics industry that is inspiring new and exciting products, as well as changing the requirements for becoming an electronics manufacturer.

American Standard Circuits Attains UL Approval for Isola's I-Tera Laminate and Prepreg Family

American Standard Circuits has obtained UL approval for the I-Tera laminate and prepreg family, which includes I-Tera MT, a very low-loss laminate engineered for high-speed digital applications made by Isola.

OM Group Satisfied with Q1 Financial Results

"The year started off as planned and first quarter results are in line with our expectations," said Joe Scaminace, chairman and CEO of OM Group. "We are making progress on our enterprise initiatives and fully expect to see benefits from these actions ramp up beginning later this year."

Innovative Circuits Installs New WISE Clean Line

Innovative Circuits, of Alpharetta, Georgia, recently installed a new Wise clean line. The Chemstar chemistry clean line will be used for surface treatment preparation of inner-layer and outer-layer panels before dry film lamination and soldermask coating.

Isola's Astra MT Materials Successfully Evaluated with Freescale Radar ICs

Isola Group, a market leader in copper-clad laminates and dielectric prepreg materials used to fabricate advanced multilayer PCBs, announced that its Astra MT laminate materials have been success-

fully evaluated with Freescale® Semiconductor radar ICs.

Commercial Avionics Systems Market Driven by Modernization

The commercial Avionics Systems Market was estimated at \$15,748.26 million in 2014, at a high CAGR of 7.06% from 2014–2020, to reach \$23,715.24 million by 2020.

OKI Technology Enables Mass Production of High-Frequency Boards

OKI Circuit Technology, an OKI group company responsible for printed circuit board business, has successfully developed design and mass production technologies for multi-layer printed circuit boards that support high speeds and high frequencies based on copper coin insertion.

Military Communications Market to Hit \$40B

Armed forces throughout the globe rely on communication systems to enable information sharing and securely stay in constant contact. The role of these systems continues to grow in importance, with new mission areas such as the control of unmanned vehicles and time-critical targeting that is heavily reliant on network connectivity.

NASA Unveils Latest Technology Roadmaps for Future Agency Needs

NASA has released the agency's 2015 technology roadmaps, laying out the promising new technologies that will help NASA achieve its aeronautics, science and human exploration missions for the next 20 years, including the agency's journey to Mars.

Global Biometrics Market Revenue to Hit \$67B by 2024

Tractica forecasts that the global biometrics market will increase from \$2.0 billion in 2015 to \$14.9 billion by 2024, with a compound annual growth rate (CAGR) of 25.3% and cumulative revenue for the 10-year period totaling \$67.8 billion.

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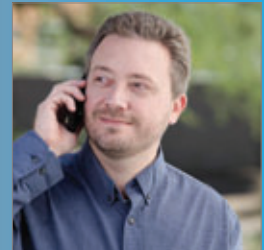
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It's Trade Show Time

by **Tim Haag**

INTERCEPT TECHNOLOGY



Like many of you, I am one of the “trade show guys” at my company. When we’re exhibiting at a trade show, I’m likely to be one of the people heading to the show to man our booth and show off our latest design software. Today is one of those days.

It’s Monday mid-morning; my work is finished and I’m packed and ready to go. I take a moment to go out to the backyard to say goodbye to my dog. True to form, he doesn’t really care that I’m going to be gone for four days, he’s only interested if I’ve brought him some sort of treat or if I am going to play with him. Since I’m doing neither, he stretches and goes back to sleep; so much for man’s best friend.

Leaving him to his nap, I hop into the truck and head to the airport. The shuttle driver taking me from the parking lot to the terminal wishes me well as I exit his van and hurry inside to the security checkpoint. Once again I am very thankful for my “known traveler number”

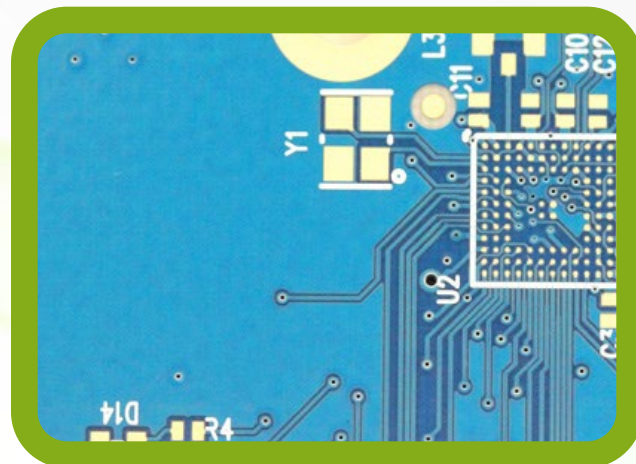
which allows me to bypass the slow-moving security line. An hour later, we are lifting off the runway and headed south. Look out Phoenix! I’m headed your way for the International Microwave Symposium, also known as IMS 2015. For companies involved in RF and microwave applications, this show is a must-attend.

The plane arrives in Phoenix after a fair amount of bumps on the way in. Not enough to make me sick, but enough to discourage a meal anytime soon. I meet up with one of my co-workers, who has just arrived, and we head out the door to find the third member of our group, the one with the rental car. The team is now complete. Since we all work in different geographical offices, there is a lot of catching up to do. What’s new with the kids? Where are you going for vacation this year? I miss these people and it is great to reconnect with them again.

Our first stop is the convention center to check in and finalize the Intercept booth setup.



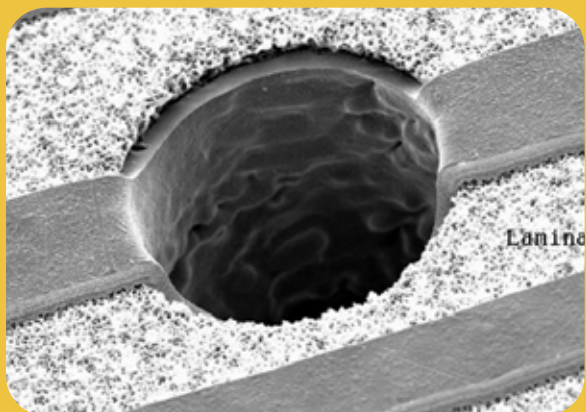
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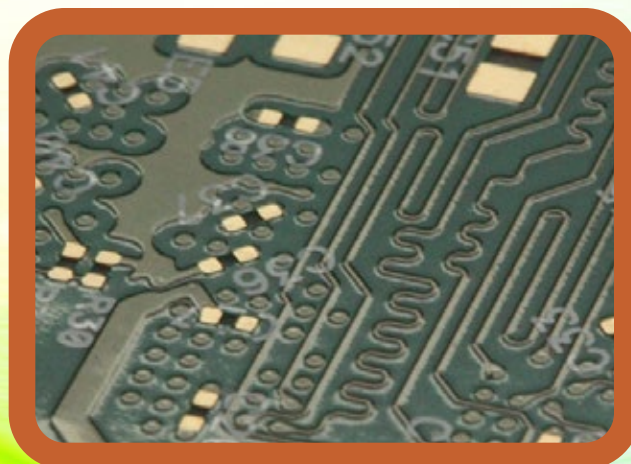


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IT'S TRADE SHOW TIME *continues*

We have a new booth this year and it's always fun to work with something new. A few tweaks here and there and we are set. Next on the agenda is dinner, and since my stomach has finally returned to a level state I am ready to sample some of the area's finest. Phoenix doesn't disappoint and we have a delicious meal before checking in to the hotel for the night. Everyone is set for the next day and the opening of the show.

The morning weather is beautiful and we strategize over breakfast. Since we are debuting some advanced functionality at this show, there's a lot to plan for and we are all pretty excited to see how it will be received. We head over to the convention center, check in and set up. Data sheets and pamphlets are laid out, the video is cranked up, and demo designs are readied to show. Bring on the show attendees, because we are ready.

At first the show traffic is light. Some of the attendees are in meeting rooms for their classes and presentations. But soon they start to filter in and we talk with them, answering their questions and showing them what's new. Since this show specializes in RF and hybrid design, we get a lot of interest in how our applications can help with these specific design scenarios. Scan a badge, exchange business cards, explain the software, and answer some questions. It's a process that will continually repeat itself throughout the three days that the exhibit hall is open.

While the show is going on, there is still regular work that needs to be attended to in the real world. So each of us will take time away from the booth to answer phone calls or e-mails and help out where we can. Yes, it can be a juggling act at times, but this is what we do. I am so proud to work with these people; they are some of the best folks in the business.

It's 5:00 pm and the first day of the show is over, but we aren't done yet. Off we go to a

meet-and-greet event. Not only does it afford the opportunity to talk shop, but we also swap stories and make new friends with people from other companies from all over the world. This event is on the rooftop of a downtown building in Phoenix and the weather was made to order. A pleasantly warm temperature combined with great food mixes in perfectly with the company and we all enjoy it.

The second day of the show is much like the first. Once again we are working with conference attendees, showing them how our applications can help them with their design needs. Some of our technology partners come by the booth, and even some of the new friends that we met last night show up. And while we are working the booth at this show, our co-workers back in the home office continue their work. These engineers are some of the greatest around and this morning they surprise us with new software enhancements that we are able to put to good use at the show.

Trade shows usually put on some sort of reception, and IMS is no exception, so as the show wraps up on the second day the convention staff starts wheeling out the trays of food and drink. A little while later we are on our way to another meet-and-greet event, and once again we have another opportunity to mingle with other people in our industry. Stories flow and still more food is served. These shows are not the most ideal time to try to lose weight!

As expected, the third and final day of the show is slower than the first two, which gives us the opportunity to roam around the show floor to see what's going on and network with other businesses. There are hundreds of booths here representing different companies and their products and services, and it is difficult to see it all. While walking around, I notice a group of 100 or more middle-school students listen-

“
It's 5:00 pm and the first day of the show is over, but we aren't done yet. Off we go to a meet-and-greet event. Not only does it afford the opportunity to talk shop, but we also swap stories and make new friends with people from other companies from all over the world.
”

ing to a presentation about future careers in the industry.

Many booths give out free samples or eye-catching novelties while others serve candy or treats, all in an attempt to get the show attendees to remember them for future business relationships. It is tempting to stock up on some of these free giveaways, but I don't want to pack it all home. (Those who pick up these tchotchkes for their kids and grandkids refer to this last lap around the show floor as the "loot run.") Later in the day a group of high school kids touring the show stop by our booth, and we talk with them about careers in software development.

And then, the show closes and it is all over. Well, it's not quite over for us; we still have to disassemble the booth and pack it up. The disassembly goes quickly but we have to wait a couple of hours for the convention staff to bring out our shipping boxes. But once that is complete we head out for our final dinner together. We enjoy another fine meal followed by the trip to the airport where we say goodbye to each other until the next show.

My flight is delayed so I have plenty of time to reflect over the last several days. The show was a success for us; we met with a lot of people and were able to show them how our software could help them with their design needs. We also spent time with our customers and busi-

ness partners and made some new friends as well.

Soon I am on the plane and headed for home. After touching down in Portland, Oregon, I retrieve my truck and drive through a lightning storm laced with heavy rain. I am worn out and happy to finally pull into my driveway. Once upstairs, I find my dog at the foot of the bed guarding my sleeping wife. The dog rolls over and gives me his "Oh, it's you" look and permits me to rub his tummy before he rolls back over and goes to sleep.

The saying "It's comforting that some things in life never change" echoes through my mind as my head hits the pillow and I too surrender to sleep. But before too long, I'll be heading to the airport for another trade show.

Let's face it: I enjoy working trades shows and meeting new people. I have a great job and I can't really complain, and no one would listen if I did! But I'm always glad to be home. **PCBDISIGN**



Tim Haag is customer support and training manager for Intercept Technology.

Trees Bear Source for High-Capacity Batteries

A method for making elastic high-capacity batteries from wood pulp was unveiled by researchers in Sweden and the US. Using nanocellulose broken down from tree fibres, a team from KTH Royal Institute of Technology and Stanford University produced an elastic, foam-like battery material that can withstand shock and stress.

"It is possible to make incredible materials from trees and cellulose," says Max Hamedi, who is a researcher at KTH and Harvard University. One benefit of the new wood-based aerogel material is that it can be used for three-dimensional structures.

The process for creating the material begins with breaking down tree fibres, making them roughly one million times thinner. The nanocellulose is dissolved, frozen and then freeze-dried so that the moisture evaporates without passing through a liquid state.

In terms of surface area, Hamedi compares the material to a pair of human lungs, which if unfurled could be spread over a football field. Similarly, a single cubic decimeter of the battery material would cover most of a football pitch, he says.

"You can press it as much as you want. While flexible and stretchable electronics already exist, the insensitivity to shock and impact are somewhat new."



Rigid-Flex PCB Right the First Time — Without Paper Dolls

by Benjamin Jordan
ALTIUM

Abstract

The biggest problem with designing rigid-flex hybrid PCBs is making sure everything will fold in the right way, while maintaining good flex-circuit stability and lifespan. The next big problem to solve is the conveyance of the design to a fabricator who will clearly understand the design intent and therefore produce exactly what the designer/engineer intended. Rigid-flex circuit boards require additional cutting and lamination stages, and more exotic materials in manufacturing; therefore, the cost of re-spins and failures are substantially higher than traditional rigid boards. To reduce the risk and costs associated with rigid-flex design and prototyping, it is desirable to model the flexible parts of the circuit in 3D CAD to ensure correct form and fit. In addition, it is necessary to provide absolutely clear documentation for manufacturing to the fabrication and assembly houses.

The traditional attempt most design teams use to mitigate these risks is to create a “paper doll” of the PCB, by printing out a 1:1 representation of the board and then folding it up to fit a sample enclosure. This presents a number of issues:

- 1) The paper doll does not also model the 3D thickness of the rigid and flex sections
- 2) The paper doll does not include 3D models of the electronic components mounted on the PCB
- 3) A physical sample of the final enclosure is needed, which may not yet be available
- 4) If the mechanical enclosure is custom designed, a costly 3D print will be required for testing. This adds much time and expense to the project. As cool as 3D printers are, it's not a sensible use for them if the modeling can be done entirely in software.

This paper discusses practical steps in two approaches to solve these problems, contrasting against the traditional paper doll approach above.

In the first scenario, a 3D MCAD model of the PCB assembly can be created in the MCAD package where a sheet metal model can be generated for the PCB substrate model. This sheet metal model can be bent into shape in the MCAD software to fit the final enclosure and check for clearance violations. This is not the best approach, but it is better than paper dolls.

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RIGID-FLEX PCB RIGHT THE FIRST TIME – WITHOUT PAPER DOLLS *continues*

In the second scenario, a significant part of the enclosure or mechanical assembly model is brought from the MCAD package into the PCB design software, where the rigid-flex board outline can be designed specifically to fit with it. Rigid-flex layer stack sections can be defined and then flexible circuit areas have bending lines added. In the PCB design tool's 3D mode, the folds are then implemented to reveal where potential clearance violations and interference occurs. The PCB design can then be interactively modified to resolve the problems and check right away—without having to build any further mock-ups or translate design databases from one tool to another.

Introduction

Rigid-flex can have ample benefits, and many designers who never had to do so before are now considering it. PCB designers are facing higher pressures to build evermore densely populated electronics, and with that come additional pressures to reduce costs and time in manufacturing. Rigid-flex PCB technology offers a solution that is viable for many product designs facing these challenges.

However, there are aspects of rigid-flex technology that could potentially be potholes in the road for newcomers. So it's wise to first understand how flex circuits and rigid-flex boards are actually made and the challenges of making sure everything will fold in the right way, all while maintaining good flex-circuit stability and lifespan.

In addition, design hand-off to the fabricator is fraught with risk, especially for those less experienced (either in design or manufacture). First, there must be absolutely clear documentation concerning what is required. Such documentation includes layer stack and material definitions, fabrication drawings, and design notes. If these items are not accurate and complete there will be production delays at best, and scrap prototypes at worst. Second, the PCB layout and design is still traditionally carried out in 2D CAD systems where it is difficult to visualize or model how the components mounted on the final PCB assembly (PCBA) will fit in 3D space when the rigid-flex circuit is in operation. Third, problems with assembly of the folded

flex circuit may not be discovered until boards are in pick-and-place (PNP) or during final prototype assembly into the target enclosure. These issues dramatically increase the risk and potential costs of developing a successful product around a rigid-flex PCB.

Rigid-Flex PCB Construction

To best understand the problems discussed in this paper it is necessary to offer a very brief overview of typical rigid-flex PCB construction. This subject matter is treated lightly here but a more thorough discussion can be found in the author's guidebook^[1].

The most common method of flexible printed circuit production is to begin with polyimide (PI) film sheets, typically 2–4 mils in thickness, which are pre-coated with laminated or electro-deposited copper foil, on one or both sides. Laminated foil is adhered to the film using a thin (typically 2 mils) adhesive layer. The copper pattern on this flexible substrate is etched using the same process as rigid PCB substrates, using a photolithographic process. Figure 1 illustrates the construction of a typical single layer flexible printed circuit (FPC). After etching, additional adhesive sheets and PI film layers are laminated onto the FPC to protect the copper, known as coverlays.

Components can be mounted on the FPC, with component land patterns (pads) being exposed for soldering through openings in the coverlay film. Thus, coverlay also forms a soldermask in most cases. Usually, the areas of the FPC that have components mounted require stiffeners, or fully rigid PCB substrate (using FR-

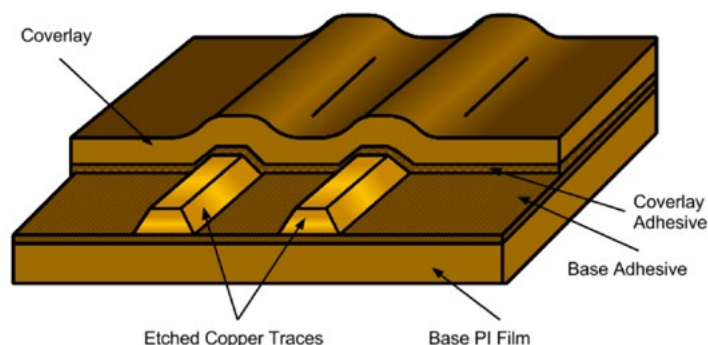


Figure 1: Single-layer FPC construction.



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RIGID-FLEX PCB RIGHT THE FIRST TIME – WITHOUT PAPER DOLLS *continues*

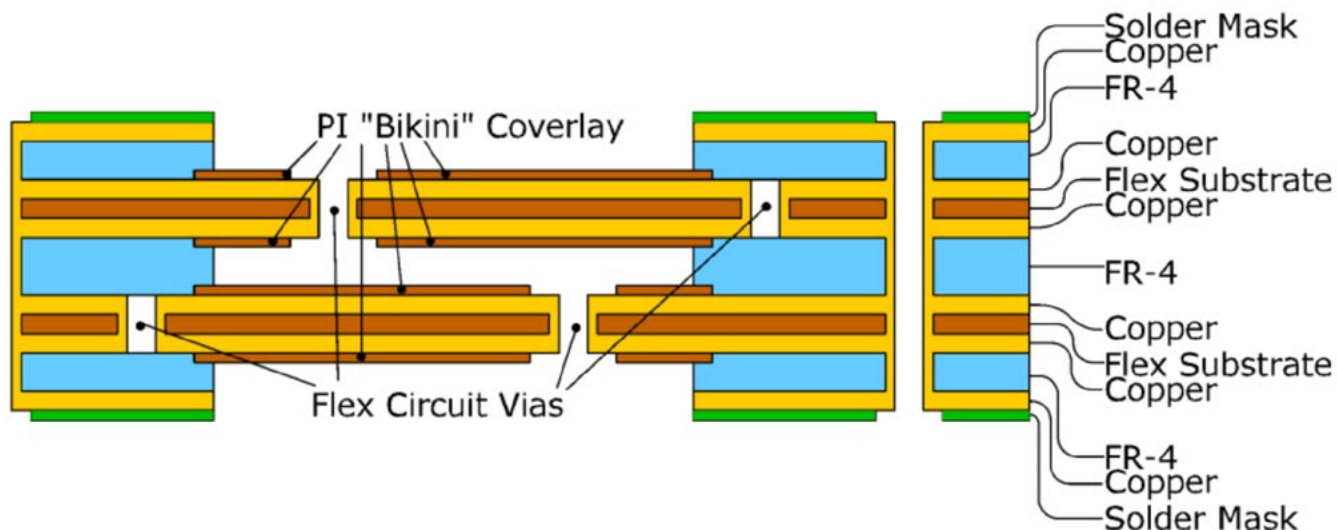


Figure 2: A typical hybrid rigid-flex layer stack cross-section.

4, for example). This gives rise to the term “rigid-flex PCB,” where some areas of the board are flexible and others are rigid where components are mounted.

The rigid sections may include additional cores, pre-pregs and copper layers or may simply have blank FR-4 or thick PI film adhered to one side as a stiffener. Figure 2 shows an illustrated cross-section of an adhesiveless rigid-flex hybrid PCB layer stack.

Author’s note: Lamination of adhesiveless boards is becoming more common, in order to avoid Z-axis expansion problems with the older adhesive-based approach. Because adhesive layers tend to expand greatly during solder reflow, they can adversely affect assembly production yield due to cracked via barrels.

The Traditional Paper Doll Approach

Design clearance issues can be mitigated using paper dolls. A paper doll is a scaled (usually 1:1) printout of the 2D PCBA outline, cut into its final shape with scissors, so named after the children’s activity of cutting a folded piece of paper into a doll shape and then unfolding it to form a string of connected doll shaped cutouts. Paper dolls have traditionally been used extensively in PCBA development, and not only for flexible electronics. Figure 3 shows an example of a typical cardboard paper doll used to model



Figure 3: PCB paper doll using cardboard, mounting posts and connectors^[2].

the mechanical fit of a carrier PCB with a daughterboard.

Immediately, one can begin to see the limitations of this approach. While it is cheaper and faster than actually building a prototype, it is extremely difficult to accurately model the entire PCBA with component interferences. One method is to glue the bulky components to the cardboard or paper so a reasonable appreciation of the 3D fit can be obtained. This is tedious and wasteful.

An example of a paper doll for a rigid-flex design is shown in Figure 4. A 1:1 printout of

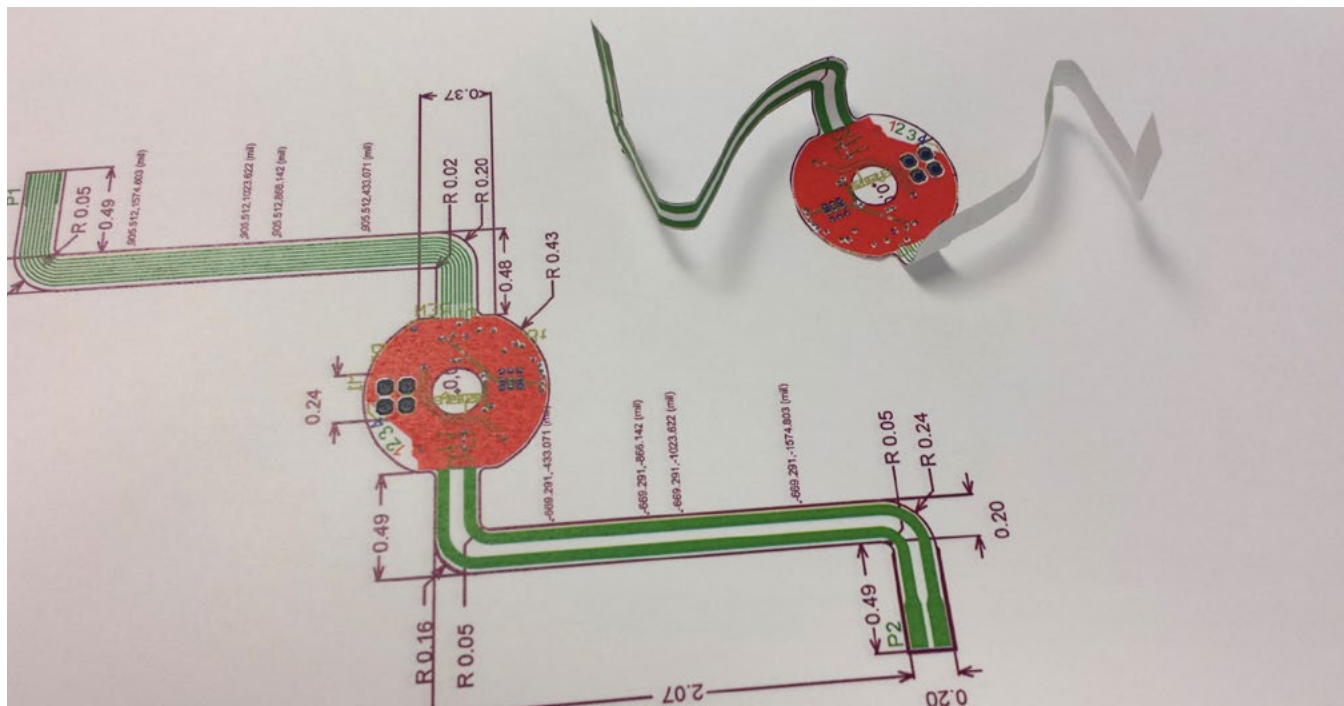


Figure 4: A paper doll of the rigid-flex design of a stepper motor controller to be mounted in a movable part of the mechanical assembly.

the PCB layout design is cut out of the paper and folded in the way that the flexible portions of the circuit should go in the final product installation. For a more accurate feel of how things will fit, cardboard which approximates the thickness of the rigid portions of the final board should be cut out and glued to the areas of the paper doll which represent the rigid areas of the design.

This approach is tedious and time-consuming, and it is very difficult to make the paper bend naturally in the same way that PI film of the final product will bend. Therefore, it's difficult to get a clear idea about the fatigue or natural folding properties of the design.

Additionally it does not allow for proper checking of the various layer stack regions, and hence there's no guarantee that the design—even if the paper doll fits and folds correctly—is actually manufacturable.

To save time and guarantee a proper fit, before the expense of costly prototypes, it is desirable to model the rigid-flex design in CAD software. Since the product is initially designed using mechanical CAD (MCAD) tools, it is not a

great deal of additional effort for skilled MCAD operators to use sheet metal models to represent the rigid-flex PCB.

Sheet Metal Model Method in MCAD

In the sheet metal method, the process is relatively straightforward but has many steps. The initial MCAD model of the product is designed along with a sheet metal component, which forms part of the assembly. One or more fixed tabs are used to model rigid sections (or flex with stiffener). Figure 5 shows a subset assembly of a product where the rigid-flex PCB substrate sits atop a stepper motor model.

This is a nice clean way of discovering what area is available for the PCB substrate, but it is still necessary to get this shape into the PCB editor's workspace. Generally, MCAD software packages that model sheet metal have an "unbend" or "unfold" feature which is usually used for generating the sheet metal stamping outputs needed for sheet metal fabrication. In this case however we need to generate a model suitable for import into the PCB editor. The unfolded sheet metal model of the board is shown in

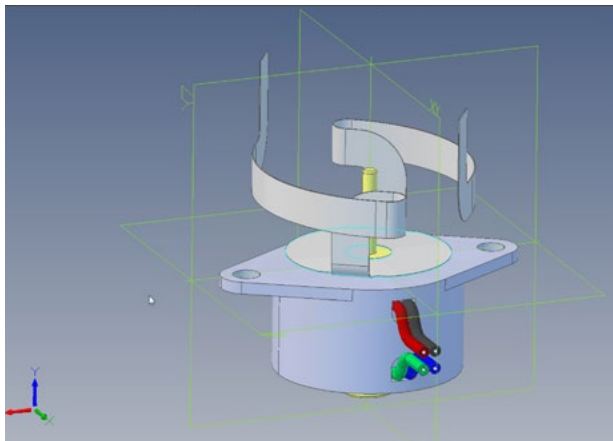
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Figure 5: Stepper motor model and rigid-flex.

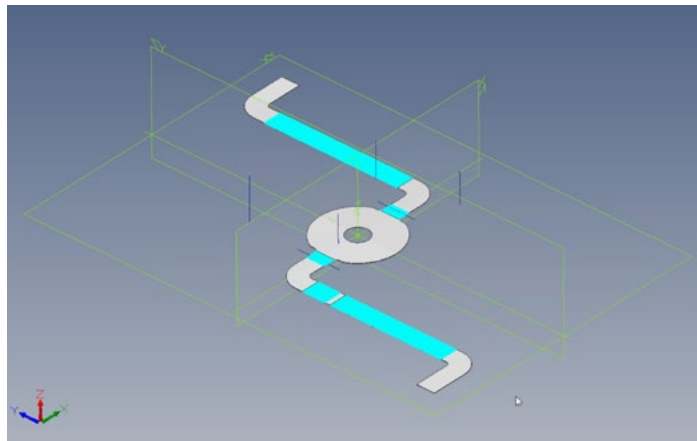


Figure 6: Here's the flattened 2D sheet metal shape to be exported to ECAD.

Figure 6 and areas subject to bending are highlighted, which can assist in planning for component placement regions known as “rooms” later on.

This sheet metal model can be exported to the PCB design software (ECAD) as either IDF or DXF in its simplest form. The PCB editor imports this board shape or outline from which the PCB shape is actually created.

Components are placed in the PCB editor and then an IDF file is generated to transmit the PCB shape and component locations back to the MCAD database, where the mechanical designer can re-fold the board substrate. However in most cases this is an unwieldy task, with some manual effort involved in maintaining the placement associations of the components on the rigid board sections in their folded positions.

The overall process involving both MCAD and ECAD domains is illustrated in Figure 7. The advantage of this method is that both mechanical and PCB design specialists get to work in their native software environments, focusing on what they do best.

Direct ECAD 3D Model

As the name suggests, in this new method the PCB layout design, rigid-flex folding design, and mechanical assembly are all modeled together directly within the ECAD software. Advancements in most modern PCB design tools enable proper 3D visualization at a minimum,

supported largely by the use of 3D STEP models of the components and mechanical enclosure or parts thereof.

ECAD software with 3D functionality is not intended to replace dedicated mechanical CAD systems. At least, not until engineering affords such a multi-disciplinary approach. Meanwhile, it is a major step forward in terms of improved workflow, and reduced waste of time and materials. High-end PCB design tools allow for Native 3D PCB design: this includes not only 3D visualization of the PCBA, but also full 3D modeling of the PCB including dielectrics and copper. Such 3D models can also be exported for thorough thermal and electromagnetic investigations.

With additional tools for native 3D modeling of the board materials, components, and mechanical object such as the enclosure, proper clearance checking and animation of flexible circuit elements is possible, offering some guarantee that the final rigid-flex design will fit in the designed enclosure and function according to specifications.

It is still beneficial for the MCAD designer to generate a 3D model of the rigid-flex board without components, and import this as a 2D outline into the ECAD software. The overall extents of the PCB are generated from this. Alternatively, this step is performed directly within the PCB design tool.

Once the PCB outline has been generated, the layer stacks for each region of the PCB de-

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December 2–4

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Shenzhen, China

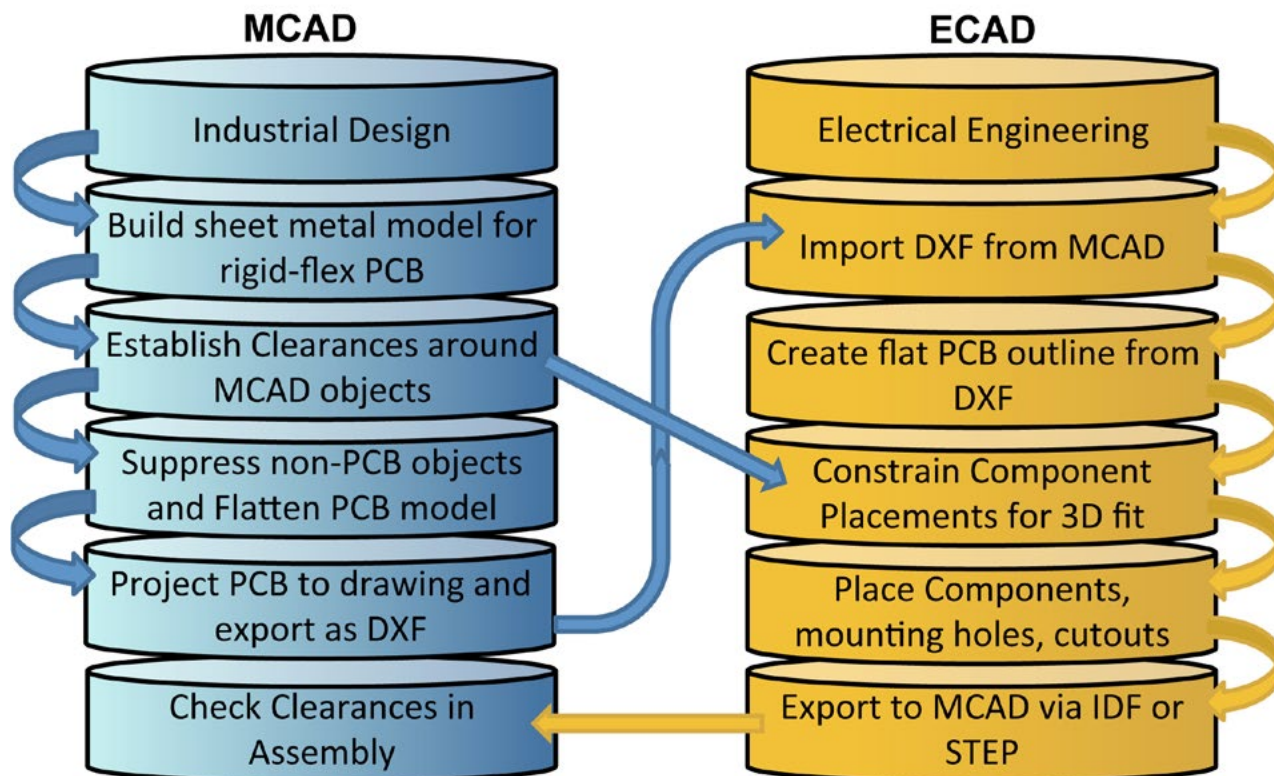
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Figure 7: Process flow with ECAD and MCAD tools having separate database.

sign (rigid and flexible) must be defined (Figure 8) and then assigned to the areas of the board that will contain those layer stack subsets (Figure 9). Once the board regions have had the various layer stacks assigned the bending and folding areas for the final product are defined also (Figure 9).

After the board regions and bending lines are defined the flex regions can be folded and examined in the software model to ensure correct form. At this stage it can quickly become apparent if the flexible extents are too short or too long and adjusted accordingly.

The components are then laid out, along with physically bulky objects with STEP models—connectors, heat sinks, LEDs, light pipes, and other parts. At this stage it is beneficial to have the final enclosure model imported into the ECAD environment using a STEP file, and interference checks can then be interactively executed in real-time, or a batch processed design rule check (DRC). Interferences can then assist in the proper relocation of components to

rapidly converge on a solution.

Figure 10 shows the 3D mode view of the sample stepper motor drive board, with flex regions folded into the in-situ shape of the final mechanical assembly. The entire PCBA file can be re-exported as a STEP model back into the MCAD software, for final mating with the mechanical design.

The modified process for rigid-flex design without paper dolls is shown in Figure 11. By enabling layer stack regions and folding simulation in the ECAD environment, final clearance/interference checking can take place visually during the design process, making it possible to do “right first time” design of rigid-flex boards every time.

At the end of the design process, further time savings are realized in that a STEP file 3D model can be generated from the entire PCBA in both folded and unfolded states, including partially folded states. This has great benefits in terms of design documentation on the MCAD side, but also allows for clear assembly

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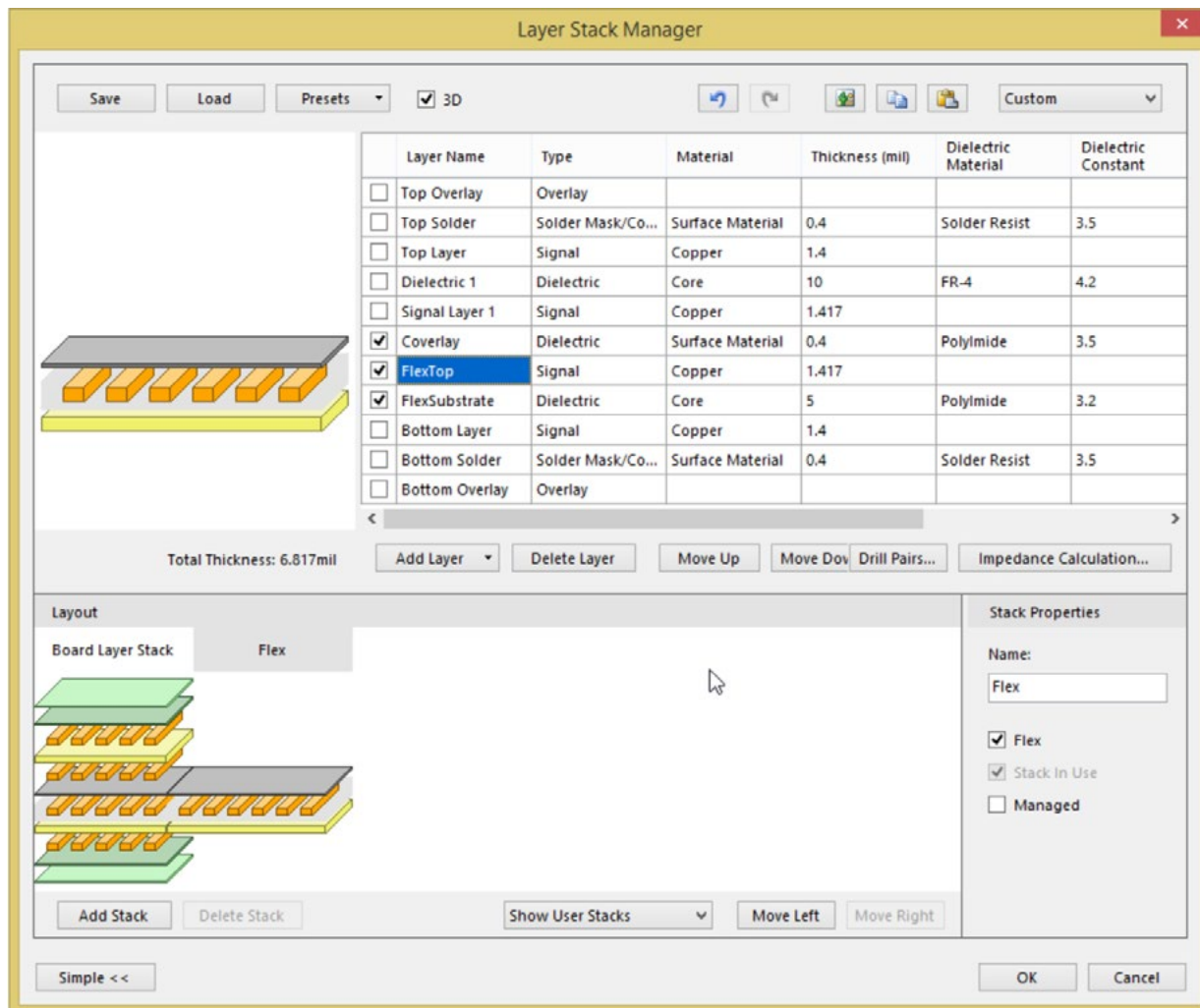


Figure 8: Layer stack definitions to be assigned to flex and rigid board regions.



Figure 9: Board regions are assigned the required layer stacks for rigid and flexible areas to be defined, and bending lines are added.

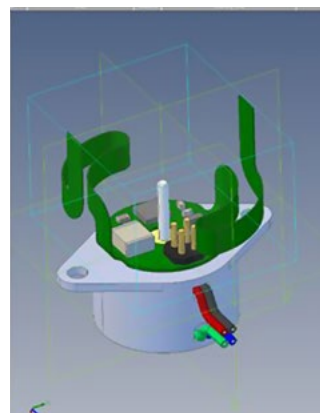
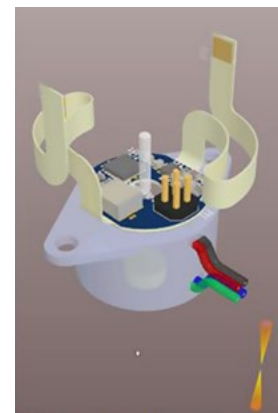


Figure 10: Native 3D model of rigid-flex and mechanical part assembly (right) and re-imported folded model of entire PCBA in MCAD software (left).



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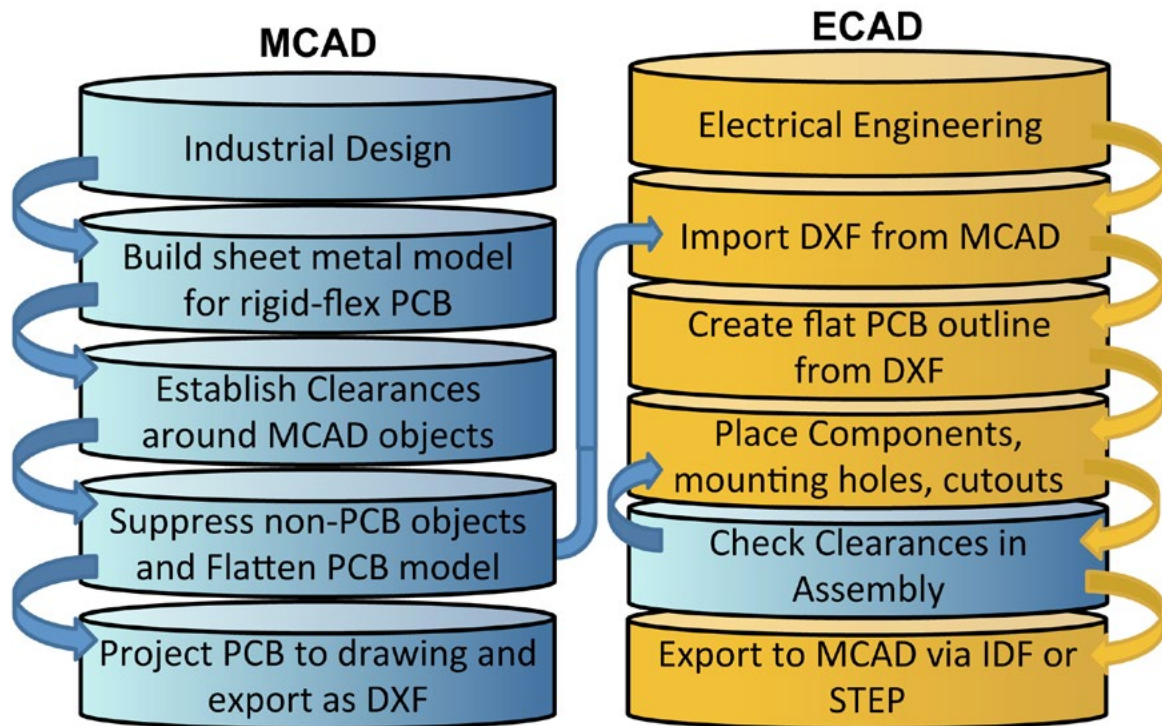


Figure 11: Streamlining the process further by performing all DFM checks in the PCB design tool.

instructions and communication of the steps to be taking during final installation of the PCBA into the product enclosure.

Using this new integrated method, at least 50% of the time normally taken to verify and validate PCB shape and folds can be saved, due to the interactive and instantaneous feedback nature of the approach.

Further time and error is reduced for final assembly, as clear images and video can be generated from the folding steps of the rigid-flex PCBA to discover the optimal assembly sequence. This video or image output can be utilized in both assembly and product service documentation. **PCBDDESIGN**

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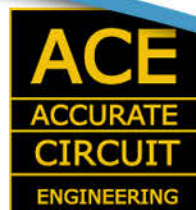
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Ben Jordan is senior product manager for PCB design and 3D modeling products at Altium.

Accurate Circuit Engineering (ACE)

Santa Ana, California, U.S.A.


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TOP TEN



Recent Highlights from PCBDesign007

1 **Mentor Graphics Unveils FloTHERM XT with EDA Connectivity**

Mentor Graphics Corporation has announced the newest version of the FloTHERM XT software product with advanced thermal management capabilities for electronic systems, printed circuit board (PCB) and packages of any geometric complexity.

That is why 22 IPC member-company executives descended on the nation's capital for IMPACT 2015: IPC on Capitol Hill, IPC's annual advocacy event.

2 **Shax Engineering: The Biggest Little Board Shop in the Bay Area**

Publisher Barry Matties recently had the chance to sit down for an interview with Isam Shakour, founder and president of Shax Engineering. This little San Jose, California company is a complete turnkey operation, providing PCB layout, fabrication, and assembly services. They discussed the company's growth since its 1998 founding, and Shakour's plans for Shax going into the future.

4 **Design Considerations: Flexible Circuit vs. Traditional PCB**

It's understandable that there are still questions about flexible circuit design vs. traditional PCB design based on the number of PCBs vs. flexible circuits manufactured worldwide, annually. However, those of us in the flexible circuit fabrication market are often asked even the simplest of questions: what kind of software do I need to design a flexible circuit?

3 **IMPACT 2015: An In-Depth Look**

IPC understands that presenting a unified voice for the electronics industry is essential for advancing policies that affect the industry's long-term future and strengthens the U.S. and global economy.

5 **Zentech Acquires Colonial Assembly & Design; Launches ZenPRO**

Zentech Manufacturing, Inc. is pleased to announce the acquisition of Colonial Assembly & Design, LLC. (CA&D). Located in Fredericksburg, Va., Colonial Assembly & Design has a thirty+ year legacy of outstanding performance in support of the Department of Defense (DOD), military primes, our nations warfighters and the commercial aviation industry.

6 Mentor Reports 1Q FY 2015 Revenues of \$272M

"The first quarter was strong for Mentor Graphics, substantially exceeding financial guidance," said Walden C. Rhines, chairman and CEO. "In addition to more than 50% bookings growth in three of our four product categories, our automotive business was very strong, driven by a major win with a leading automotive OEM. We also initiated a strategic and geographic realignment of resources. First quarter results provide a solid start to the year."

7 Cadence Strengthens Allegro Technology Portfolio

Cadence Design Systems, Inc., has unveiled the Allegro 16.6 portfolio, which features several new products and technologies. Included in this release is the new Allegro PCB Designer Manufacturing Option, which can shorten the time to create manufacturing documentation by up to 60 percent, and several key technology updates catered to increase efficiency, control and productivity for designers.

8 Material Witness: How About that Technical Roadmap!

You may remember the movie What About Bob? If you do, you may recall the scene in which Bob

(played by Bill Murray) confronts his psychiatrist (played by Richard Dreyfuss) and emotes, "I need! I need! I need! Gimme! Gimme! Gimme!" It's tough figuring out how to make PCB materials that meet all the "I need!" and "Gimme!" requirements in this industry.

9 Intercept Enhances Advanced Design System Interface Functionality

Intercept Technology Inc., a leading EDA software developer for PCB, RF and hybrid design solutions, has announced enhancements to the Keysight Technologies Advanced Design Systems (ADS) Board Link interface functionality within Pantheon.

10 Pulsonix and Ucamco Collaborate to Fully Integrate Gerber X2 in Pulsonix 8.5

WestDev Ltd., the EDA company delivering technology-leading PCB design solutions, has announced the completion of its Gerber X2 output. Working closely with Ucamco, the developer of the Gerber format, Pulsonix has successfully implemented Gerber X2. The output has been fully verified by Ucamco, who confirm it conforms to the X2 specification.

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June 18, 2015
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[Symposium on Counterfeit Parts and Materials—Tabletop Exhibition](#)

June 23–24, 2015
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PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:

PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA,
TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

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September:
**Cars: A Driving
Force in the
Electronics
Industry**